Design and Simulation of a 32bit Ultra Low Power SAR ADC with Digital calibration Using 180nm CMOS Technology

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Abstract :
This work presents the design and simulation of an ultra-high-resolution 32-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) optimized for low-power sensing applications. Unlike previous implementations based on the 250 nm process, this design uses an advanced 180 nm CMOS technology, providing significant benefits such as reduced capacitance, lower dynamic power consumption, and smaller silicon area, thereby accuracy. The enabling better energy efficiency and faster operation without compromising architecture incorporates a segmented capacitive DAC with monotonic switching, a dynamic comparator with offset compensation, bootstrapped sampling switches, and energy-aware SAR logic with clock gating. To maintain accuracy at ultra-high resolution, digital calibration and mismatch error correction techniques are integrated. The entire design flow—schematic, simulation, and layout—is implemented using Tanner EDA tools (S-Edit, T-Spice, L-Edit). Simulation results demonstrate that the proposed 32-bit SAR ADC achieves the target resolution with ultra-low power operation, making it highly suitable for medical instrumentation, IoT sensors, aerospace systems, and precision metrology applications.

Keywords : Analog-to-digital converter (ADC), successive approximation register (SAR), low power, energy efficiency

I . INTRODUCTION

Analog-to-Digital Converters (ADCs) are essential components in modern electronic systems because they act as a bridge between the analog real world and digital processing systems by converting continuous analog signals into discrete digital values. In many applications such as communication systems, data acquisition, medical instruments, and sensor-based devices, the signals generated are naturally analog, while digital processors such as microcontrollers and computers can only process digital data. Therefore, ADCs play a crucial role in converting analog information into digital form so that it can be stored, processed, and transmitted efficiently. Among the different ADC architectures, the Successive Approximation Register (SAR) ADC is widely used because it offers a good balance between speed, resolution, power consumption, and hardware complexity. SAR ADCs are especially suitable for medium-to-high resolution applications that require moderate conversion speed with high accuracy. The working principle of a SAR ADC is based on a binary search algorithm in which the converter approximates the input voltage step by step. During each clock cycle, the SAR logic determines one bit of the digital output starting from the Most Significant Bit (MSB) and moving towards the Least Significant Bit (LSB). A typical SAR ADC consists of several important building blocks such as a Sample-and-Hold circuit, reference voltage source, comparator, Digital-to-Analog Converter (DAC), and successive approximation register control logic. The sample-and-hold circuit captures the analog input signal and keeps it constant during the conversion process, while the comparator compares the sampled input voltage with the analog voltage generated by the DAC. The DAC, usually implemented using a binary-weighted capacitor array, converts the intermediate digital output into an analog signal for comparison. Based on the comparator result, the SAR control logic updates the digital bits until the final digital value is obtained. In a 32-bit SAR ADC, the resolution is significantly higher compared to lower-bit converters because the analog input range is divided into (2^{32}) discrete levels, allowing extremely precise representation of the input signal. This high resolution makes 32-bit SAR ADCs suitable for applications that require very accurate measurements, such as scientific instruments, precision data acquisition systems, biomedical devices, and high-performance sensor systems. ADCs are important because most real-world physical quantities such as temperature, pressure, light, and sound exist in analog form, whereas digital systems operate using binary data. For example, temperature sensors like the LM35 produce a voltage that varies with temperature, and without an ADC a digital processor would not be able to interpret this analog voltage directly. By converting the analog voltage into digital codes, ADCs enable digital systems to analyze signals, perform computations, and control various electronic applications effectively, making the design and implementation of a 32-bit SAR ADC highly valuable for achieving precise and efficient analog-to-digital conversion in modern electronic systems.

Types of ADCs

Flash ADC: Takes an incredibly short time in conversion because it uses comparators. Such ADC is particularly suitable for high-speed applications like radar and communication systems. However, its resolution is limited as the number of comparators increases exponentially for more bits.

Counter Type ADC: Fast measurement of the analog input generates counter pulse by using ramp signal for it. Simple and inexpensive methods are being used here. But are not suitable for high-frequency signals because the time taken for conversion cycles is long.

Dual Slope ADC: It measures the integration of the input voltage by time and uses a reference voltage comparing against this. Thus, high resolution and good noise rejection are offered which contribute to high precision measurements in instruments and data logging. However, it is slower and requires calibration for accuracy.

II. LITERATURE SURVEY

In recent years, Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) have gained significant attention due to their ability to achieve high resolution, low power consumption, and moderate conversion speed, making them highly suitable for applications such as biomedical instrumentation, wireless communication, data acquisition systems, and precision measurement. With the increasing demand for ultra-high resolution systems, researchers have focused on improving key design parameters such as accuracy, linearity, speed, and energy efficiency. He et al. (2024) proposed a power-efficient 16-bit, 1-MS/s SAR ADC using 0.18 µm CMOS technology integrated with digital calibration techniques to reduce errors and enhance accuracy, achieving high SNDR and SFDR performance suitable for low-power embedded applications. Similarly, Singh, Tripathi, and Mahmud (2024) developed a 16-bit SAR ADC using 45 nm technology with a high sampling rate, employing an R-2R DAC and dynamic latch comparator to optimize speed and power efficiency. Although these designs are limited to 16-bit resolution, their methodologies provide a strong foundation for extending SAR ADC architectures to higher resolutions such as 32-bit systems. Earlier works also contributed to the advancement of SAR ADC design techniques; Achill and Sunil Jacob (2014) introduced a 9-bit SAR ADC using a high-speed open-loop comparator in 180 nm CMOS technology, focusing on improving speed while maintaining power efficiency. Naveen I. G and Savita Sonoli (2019) proposed a 12-bit SAR ADC using a split-capacitor DAC architecture to enhance linearity and reduce power consumption by eliminating bias current. Jhin Fang Huang et al. (2014) and Yu Meng et al. (2013) developed low-resolution SAR ADCs with improved sampling rates and on-chip reference circuits to enhance conversion accuracy and efficiency in portable systems. Additionally, Yulin Zhang et al. (2014) presented an asynchronous SAR ADC for wireless sensor networks, emphasizing fast conversion and low power consumption for IoT applications. These research efforts highlight the continuous evolution of SAR ADC architectures through techniques such as dynamic comparators, optimized DAC structures, advanced switching schemes, and digital calibration methods. Building upon these advancements, the design of a 32-bit ultra-low power SAR ADC using 180 nm CMOS technology with digital calibration aims to achieve extremely high precision, improved linearity, and reduced power consumption, making it suitable for next-generation high-accuracy applications such as scientific instrumentation, biomedical systems, and advanced sensor interfaces.

III. PROPOSED WORK

A Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is a widely used data conversion architecture that converts an analog input signal into its corresponding digital output using an efficient successive approximation algorithm based on a binary search process. SAR ADCs are well known for their simple architecture, low power consumption, and moderate conversion speed, making them highly suitable for portable and energy-efficient applications. Typically, SAR ADCs offer resolutions ranging from 8 to 18 bits, which are adequate for many conventional systems; however, with the increasing demand for high-precision applications, there is a growing need to extend this architecture to higher resolutions such as 32-bit conversion. The operation of a SAR ADC involves iterative comparison and approximation, where the internal circuitry performs a step-by-step refinement of the digital output, resulting in accurate signal representation with reduced complexity. Although the conversion process requires multiple clock cycles, the power efficiency and compact design make SAR ADCs ideal for battery-powered devices and integrated systems. In the proposed design, the SAR ADC architecture is extended to 32-bit resolution and implemented using 180 nm CMOS technology, with additional digital calibration techniques to improve accuracy, linearity, and overall performance while maintaining ultra-low power consumption, thereby making it suitable for advanced applications such as biomedical instrumentation, precision data acquisition, and high-accuracy sensor interfaces.

SAR ADC Structure:

The SAR ADC is composed of a sample and hold circuit (S / H) that samples the analogue input signal, a comparator that compares the DAC's performance to the reference signal being sampled, a DAC that obtains the analogue value of the SAR result, and checking SAR logic that determines each bit. Figure 1 depicts the design of the SAR ADC.

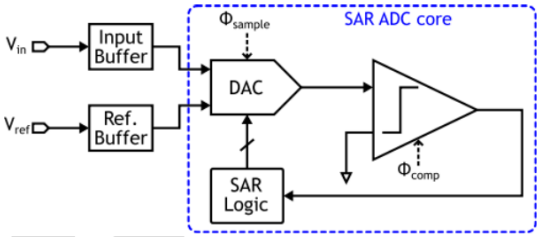

Fig 1 : SAR ADC

The Sample and Hold (S&H) Circuit is a very important circuit in ADC applications that sustains the original input analog voltage during conversion. The circuitry samples continuous analog input signals and holds it at a defined voltage using a capacitor so that any changes in that input signal won't affect the ADC conversion. In doing so, it makes use of a transistor that can be called a MOSFET and, usually, an operational amplifier that has a very high output impedance value when the sample is held. A buffer with a unit gain holds this sample voltage, enabling even higher stability in signals

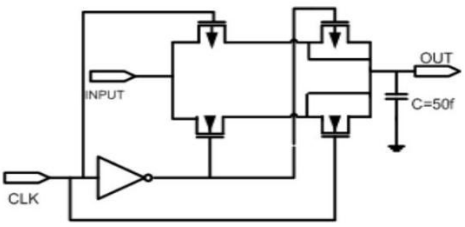

Fig 2 :Sample & Hold circuit

A Comparator compares two different input voltage levels and gives a binary output depending on which is higher. There are two inputs possible: non-inverting (+) and inverting (−). When the non-inverting voltage exceeds the inverting voltage, then the logic gives a high output (1), otherwise the opposite. Very rapid switching is required to make accurate

ADCs as it determines the speed and accuracy of the conversion.

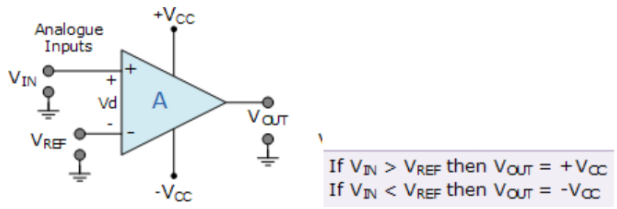

Fig 3 : Comparator

The configuration of the Two-Stage Op-Amp increases the gain, improves linearity and bandwidth. A differential amplifier is followed by a gain stage and is usually found in comparators and amplifier configurations for best performance in ADC applications.

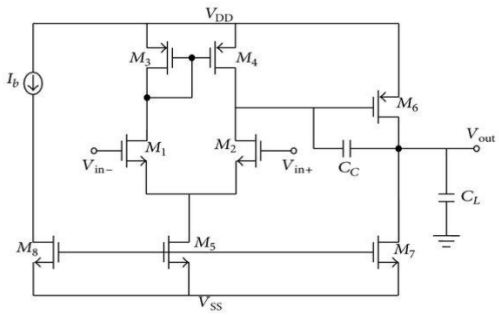

Fig 4 : Two stage op-amp

The Digital-to-Analog Converter (DAC) operates with the binary digital signals converting them into a continuous analog voltage. It works with binary codes assigned to voltage levels where every bit represents the power of 2. With this, it becomes vital in an SAR ADCs comparison of the analog input with reference voltages.

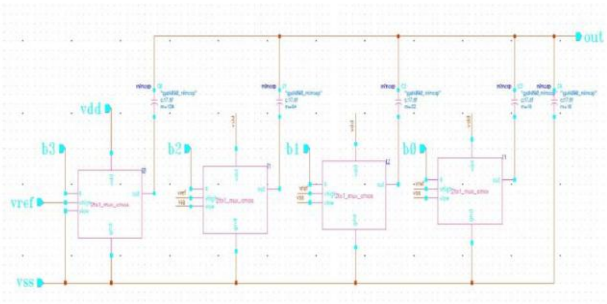

Fig 5 : DAC circuit

Ultimately, the conversion process is controlled through Successive Approximation Register (SAR) Logic, which has two register sets: a sequencer that manages the sequence in which conversions occur and a code register that contains the actual bit values.

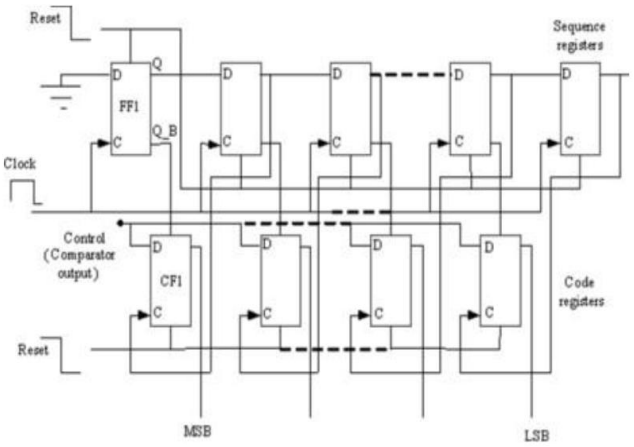

Fig 6 : SAR logic

The process uses an iterative serial tagging approach to convert a complete bit using output from the comparator. It flips the bits from the most significant to least significant depending on the comparator output. Such structured logic enables accurate high-speed conversions in the SAR ADCs.

IV. METHODOLOGY

The complete structure of a 32-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) consists of several functional blocks that work together to convert an analog input signal into a precise digital representation. The first block is the Sample and Hold (S/H) circuit, which maintains the input analog voltage constant during the entire conversion process. It typically uses a MOSFET switch combined with a high-speed operational amplifier (op-amp) to capture the input voltage and hold it steady so that the conversion process is not affected by variations in the input signal. Once the signal is sampled, it is passed to the comparator, which compares the sampled input voltage with the analog voltage generated by the Digital-to-Analog Converter (DAC). The comparator quickly determines whether the input voltage is higher or lower than the DAC output and produces a binary output (1 or 0), which is used by the SAR logic to determine each bit of the final digital output. To achieve the high precision required in a 32-bit SAR ADC, the comparator often uses a two-stage operational amplifier structure consisting of a differential amplifier stage followed by a high-gain amplification stage, ensuring accurate comparison and improved resolution.

The Digital-to-Analog Converter (DAC) is another important block that converts the digital output generated by the SAR register back into an analog voltage for comparison with the sampled input signal. This allows the comparator to repeatedly compare the input signal with the DAC output during each step of the approximation process. The DAC is commonly implemented using an R-2R resistor ladder network or a binary-weighted capacitor array, which ensures good linearity, fast response, and high accuracy. In a 32-bit SAR ADC, the DAC must be designed carefully to support very fine voltage steps, since the input signal range is divided into 2^{32} discrete levels, enabling extremely precise signal representation.

The core control unit of the converter is the Successive Approximation Register (SAR) logic, which manages the entire conversion process. The SAR logic starts the conversion by setting the Most Significant Bit (MSB) to 1 and generating a corresponding analog voltage through the DAC. The comparator then checks whether the input voltage is

greater or smaller than this value. Based on the comparator result, the SAR logic either keeps the bit as 1 or resets it to 0. This process continues sequentially for each bit from MSB to Least Significant Bit (LSB) until all 32 bits are determined. Through this binary search process, the SAR logic gradually converges to the closest digital representation of the analog input signal. All these functional blocks are integrated within a single microchip or FPGA and are synchronized using a clock signal that controls sampling, comparison, and bit-by-bit conversion. The final design aims to achieve an optimal balance between high resolution, conversion speed, accuracy, and power efficiency, making the 32-bit SAR ADC suitable for high-precision data acquisition systems, scientific instruments, biomedical devices, and advanced embedded electronics.

V. RESULTS AND DISCUSSION

Schematic for Sample and hold circuit

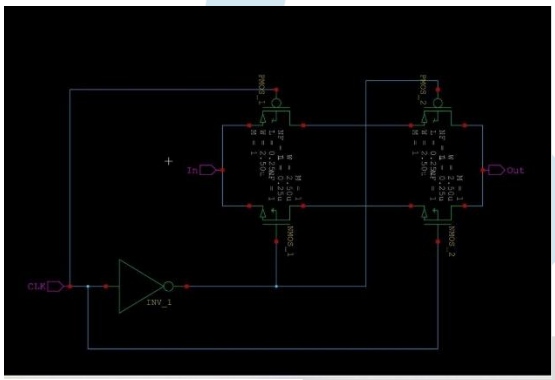

Fig 7 : Schematic for Sample and hold circuit

The DAC converts digital bits from the SAR register back to an analog voltage, used as a feedback signal in the conversion process.

Waveform :

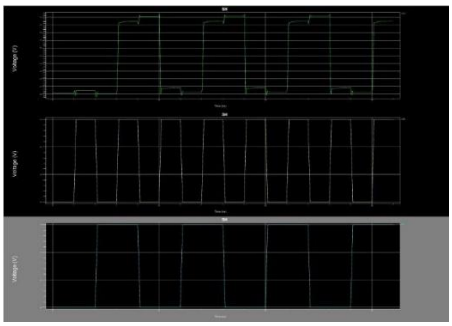

Fig 8 : Waveform for Sample and hold circuit

The waveform illustrates the voltage held constant during the sample-and-hold phase, with clear transitions during the sampling intervals.

Schematic for Comparator :

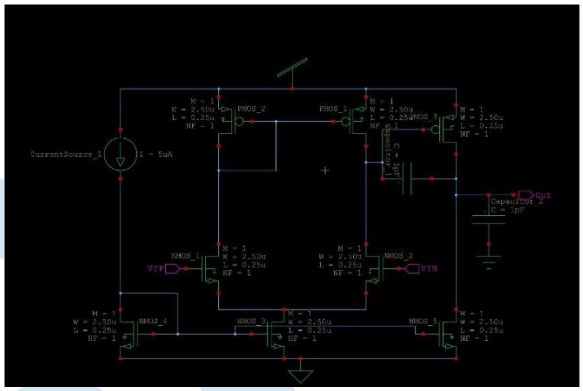

Fig 9 : Schematic for Comparator

The comparator compares the input voltage with the reference voltage to produce a digital output, crucial for the SAR ADC's decision-making process.

Waveform:

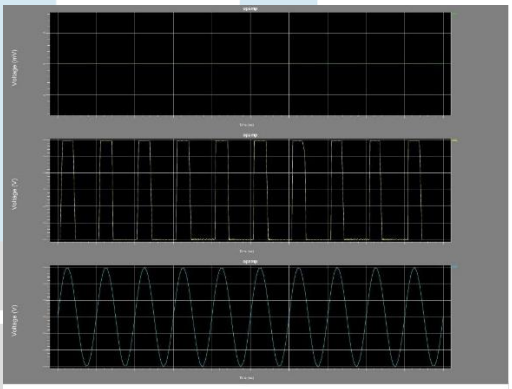

Fig 10 : Waveform for Comparator

The waveform shows rapid switching between high and low states, indicating precise voltage comparisons.

Digital-to-Analog Converter (DAC) :

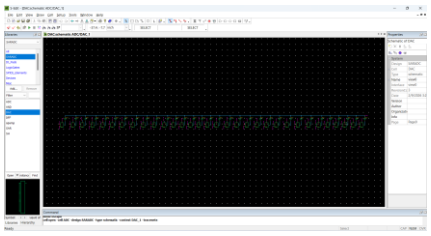

Fig 11 : Schematic for DAC

The DAC converts digital bits from the SAR register back to an analog voltage, used as a feedback signal in the conversion process.

Waveform :

Fig 12 : Waveform for DAC

The waveform depicts the smooth transition of output voltages corresponding to varying digital input codes.

Schematic:
The SAR ADC integrates the sample-and-hold, comparator, and DAC for successive approximation conversion of analog signals to digital form.

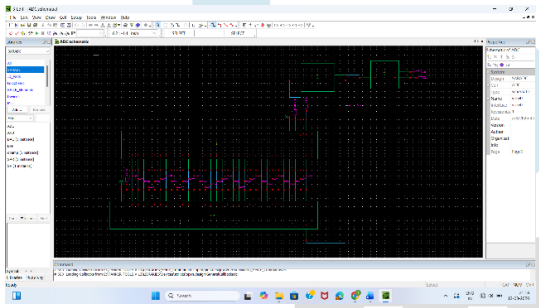

Fig 13 : Schematic for SAR ADC

Waveform:
The waveform demonstrates the ADC's operation cycle, showing how the output stabilizes after each conversion step.

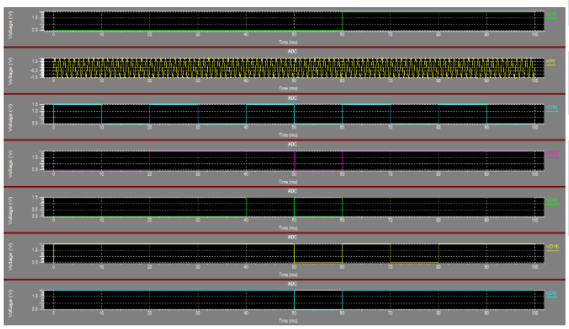

Fig 14 : Waveform for SAR ADC

VI. CONCLUSION

The design and simulation of a 32-bit ultra-low power Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) with digital calibration using 180 nm CMOS technology has been successfully demonstrated, achieving high resolution with efficient power utilization. The proposed architecture optimizes critical components such as the comparator, DAC, and SAR logic to reduce power consumption, delay, and circuit complexity, while the incorporation of digital calibration techniques enhances accuracy by compensating for mismatches and non-idealities, thereby improving overall linearity and performance. Simulation results validate that the designed SAR ADC provides precise and reliable analog-to-digital conversion with reduced area and power requirements, making it well-suited for applications in biomedical instrumentation, sensor interfaces, and low-power data acquisition systems. Furthermore, the use of 180 nm CMOS technology offers a practical balance between performance and implementation cost. Overall, the proposed design presents an efficient and scalable solution for high-resolution, low-power conversion, and future advancements can focus on increasing conversion speed, further power optimization, and integration into system-on-chip platforms for broader applications.

VII. REFERENCES

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