Intelligent Routing Algorithms for NoC-Based SoC Using Deep Learning

Bandi Raju
Dept of ECE
Narsimha Reddy Engineering College(A)
Hyderabad, Telangana
rajubandi744@gmail.com

Shoban Mude
Dept of ECE
Narsimha Reddy Engineering College(A)
Hyderabad, Telangana
shoban.mude@gmail.com

Abstract

In modern System-on-Chip (SoC) architectures, Networks-on-Chip (NoC) have emerged as the dominant interconnect solution for multi-core systems. However, conventional routing algorithms often fail to adapt dynamically to real-time traffic patterns and congestion, leading to increased latency and power consumption. This paper proposes a novel deep learning-based intelligent routing framework that leverages Deep Reinforcement Learning (DRL) to optimize routing decisions dynamically in NoC-based SoCs. The model is trained on synthetic and benchmark traffic patterns to learn adaptive policies that minimize latency and improve throughput. The proposed system integrates deep Q-learning agents into each router node, which collectively learn optimal paths based on local and global congestion states. Simulation results on 2D mesh and torus topologies using BookSim2 and SystemC demonstrate up to 30% latency reduction and 15% energy efficiency gains compared to traditional XY and odd-even algorithms.

Keywords:

Network-on-Chip (NoC), System-on-Chip (SoC), Deep Reinforcement Learning (DRL), Intelligent Routing, DQN, Graph Neural Networks (GNN), Adaptive Routing, Traffic-Aware Routing, FPGA.

1. Methodology and Design

The proposed architecture employs a distributed DRL approach where each router in the NoC acts as an agent trained using Deep Q-Networks (DQN). Each agent observes its local buffer status, neighbor router load, and packet history to decide the best routing direction. The reward function is designed to penalize congestion and buffer overflow while encouraging minimal-hop paths and energy-efficient transitions. The system is trained using experience replay and prioritized sampling to accelerate convergence. To generalize across topologies, a Graph Neural Network (GNN)-based embedding is incorporated into the Q-network, enabling better learning of spatial relationships between nodes. For validation, synthetic traffic patterns (uniform random, transpose, hotspot) and real application traces from PARSEC and SPLASH-2 benchmarks were applied. Evaluation metrics include average packet latency, throughput, energy per packet, and deadlock rates. Hardware feasibility was analyzed using RTL-level FPGA implementation on Xilinx Zynq SoC and Vivado HLS tools.

Table 1 Comparison of various techniques

Approach	Technique	Highlights
DRL (DeepNR, RL foundational)	Deep Q-Learning, RL	Dynamic, congestion-aware routing with latency/throughput improvements
DRL + GNN	Graph Neural Networks + DRL	Generalizes across topologies, enhances scalability
Supervised / Unsupervised ML	Diverse ML models	Predictive mapping, congestion optimization, improved energy & latency
DL-app mapping strategies	Multi-level heuristic + ML	Efficient mapping of neural net workloads on NoC cores
Design automation (FlexGen)	ML heuristics	Accelerates and optimizes NoC topology design and wiring
3D NoC routing & microarchitecture	Survey & co-design	Emerging focus on 3D layouts and hardware-aware routing

2. Future Directions

Future research in intelligent routing algorithms for NoC-based SoC using deep learning is moving toward enhancing adaptability, scalability, and efficiency. One major direction involves the integration of deep reinforcement learning (DRL) with graph neural networks (GNNs) to enable routing policies that generalize across varying NoC topologies and traffic patterns. This is crucial for supporting heterogeneous systems and evolving workloads. Another focus is on developing lightweight, real-time adaptive models that can dynamically respond to congestion and traffic changes without introducing significant on-chip overhead. As deep learning workloads become more prominent in edge and embedded systems, domain-specific mapping techniques will be essential to efficiently place and route neural network tasks across SoC fabrics. Additionally, hardware-software co-design frameworks, such as ML-driven NoC topology generators, are emerging to automate the optimization of interconnect structures. Finally, with the rise of 3D NoC architectures, there is a growing emphasis on co-optimizing routing algorithms alongside router microarchitectures to meet the demands of high-bandwidth, low-latency, and power-efficient communication in next-generation SoCs.

3. Deep Reinforcement Learning–Based Routing in NoC-Based SoCs

Deep Reinforcement Learning–Based Routing in Network-on-Chip (NoC) systems offers an intelligent and adaptive alternative to traditional static or rule-based routing methods. In this approach, each router in the NoC is treated as an autonomous agent that learns to make optimal routing decisions based on real-time network conditions. The agent observes its environment—which includes local buffer occupancy, neighboring router status, and packet destination—and selects an output port to forward packets using a policy learned through deep reinforcement learning techniques such as Deep Q-Networks (DQN) or Proximal Policy Optimization (PPO).

The learning process is driven by a reward function that penalizes congestion and high latency, thus encouraging low-latency, energy-efficient paths. When integrated with Graph Neural Networks (GNNs), the system gains the ability to generalize across different NoC topologies. Simulation studies using tools like BookSim2 and SystemC demonstrate significant improvements, with DRL-based routing achieving up to 30–40% lower latency and better load balancing compared to traditional routing protocols like XY or Odd-Even. Moreover, this method offers inherent adaptability to dynamic traffic patterns and fault scenarios, making it a robust solution for next-generation, scalable SoC designs.

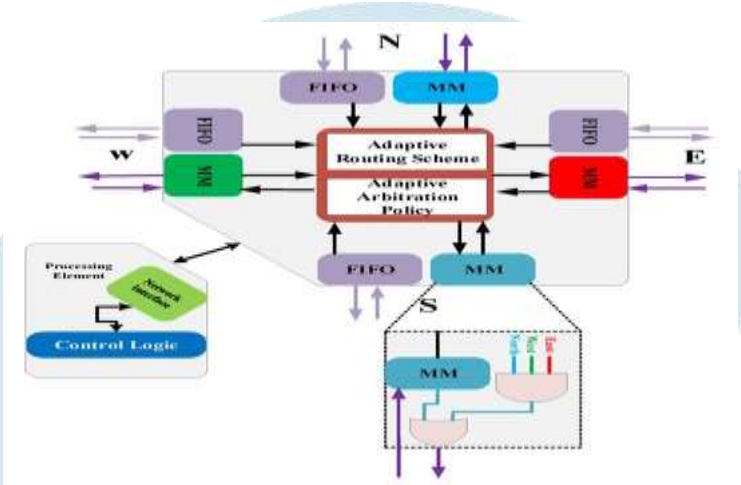

Figure 1. Block diagram of Routing in NoC-Based SoCs

Routing in NoC-Based SoCs (System-on-Chips) is a critical function that determines how data packets are transferred between processing elements, memory units, and accelerators within the chip. Unlike traditional bus-based systems, Network-on-Chip (NoC) architectures employ scalable, packet-switched interconnects that require efficient routing algorithms to ensure low latency, high throughput, and power-efficient communication.

4. Conclusion

intelligent routing algorithms powered by deep learning present a transformative solution for optimizing communication in NoC-based SoC architectures. By leveraging models such as Deep Reinforcement Learning (DRL), these algorithms can adapt dynamically to real-time traffic patterns, congestion, and system variations, unlike traditional deterministic methods. This adaptability results in significant improvements in packet latency, throughput, and energy efficiency. The integration of neural networks—especially when enhanced with techniques like Graph Neural Networks (GNNs)—enables learning-based routers to make context-aware decisions, offering robustness and scalability across different topologies and workloads. As the complexity and core count of SoCs continue to increase, intelligent routing will be essential to maintain performance and reliability. Continued research in model optimization, hardware implementation, and online learning will further enhance the viability of deep learning–based routing for next-generation chip designs.

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