GDI NOR Logic and half adder fusion using PASTA logic

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Abstract**—**The design and implementation of GDI NOR logic are examined in this project, along with how it may be fused with a half-adder using PASTA logic and then extended to a full-adder using the GDI approach. With fewer transistors and better performance, GDI (Gate Diffusion Input) provides a power-efficient substitute for traditional CMOS logic. Asynchronous addition is made possible using PASTA (Parallel Self-Timed Adder) logic, which improves speed and power efficiency. Using Cadence software, the research puts these designs into practice while examining important performance indicators including area, power consumption, and delay. The findings show that GDI-based designs perform better than traditional techniques in terms of compactness and energy efficiency. The study lays the groundwork for future investigations into intricate arithmetic circuits utilizing GDI and PASTA approaches while also advancing low-power VLSI design

Keywords— GDI Logic, PASTA, Low-Power Design, Full Adder, Half-Adder, VLSI, Cadence Simulation

I. Introduction

As the demand for low-power, high-performance digital circuits continues to rise, researchers and engineers are actively exploring innovative design methodologies to enhance power efficiency, optimize area usage, and improve speed. Gate Diffusion Input (GDI) technology has emerged as a viable solution to minimize power consumption and reduce the number of transistors while preserving the logical functionality of conventional CMOS logic. This approach is particularly advantageous for developing low-power arithmetic circuits, which are critical in processors, communication systems, and embedded applications. Traditional CMOS logic circuits encounter various challenges, such as significant power dissipation, an increased number of transistors, and substantial silicon area requirements. GDI logic addresses these issues by altering the diffusion inputs of transistors, allowing for the realization of complex functions with fewer components. This makes GDI an attractive option for power-sensitive applications, including battery-operated devices and portable systems. A key element in arithmetic logic design is the adder circuit, which serves as the foundational component for multipliers, subtractors, and Arithmetic Logic Units (ALUs). Conventional adders, like Ripple Carry Adders (RCA) and Carry Lookahead Adders (CLA), often experience high power consumption and delays. To mitigate these problems, the PASTA (Parallel Self-Timed Adder) logic has been introduced as an asynchronous method that enhances speed and power efficiency. This project aims to investigate a novel integration of GDI NOR logic with a Half-Adder and extend it to a Full-Adder using GDI technology. The study will implement and assess the performance of GDI-based NOR gates, Half-Adders, and Full-Adders, focusing on power consumption, delay, and area. Cadence simulation tools will be employed to compare the efficiency of these circuits against traditional CMOS-based designs.

II. LITERATURE SURVEY

As the demand for low-power digital circuits rises, researchers have explored alternatives to conventional CMOS logic, with Gate Diffusion Input (GDI) emerging as a promising approach. GDI allows complex logic functions with fewer transistors, reducing power consumption and area while maintaining functionality [14]. Studies show that GDI-based gates, including NOR, NAND, and XOR, require fewer transistors and exhibit lower power dissipation compared to CMOS counterparts [15]. GDI's efficiency in arithmetic circuits such as adders and multipliers has been validated [14], while its use in multiplexers minimizes power and area overheads [10]. A modified GDI (MGDI) approach further enhances efficiency, outperforming traditional CMOS and GDI designs in deep-submicron nodes [16]. Low-power GDI-based full adders achieve up to 40% power reduction [10]. Traditional adders, including Ripple Carry and Carry Lookahead Adders, suffer from high power and delay, making Parallel Self-Timed Adder (PASTA) logic a suitable asynchronous alternative [3]. PASTA logic eliminates global clocks, improving speed and reducing power. Integrating PASTA with GDI enhances low-power arithmetic circuits, particularly in asynchronous applications [5]. GDI-based adders outperform CMOS designs in power and delay [13], and studies confirm that FinFET-based GDI full adders achieve a better power-delay product than CMOS [5]. Cadence Virtuoso simulations validate GDI's effectiveness, confirming enhanced power efficiency [18]. Research shows GDI is suitable for ultra-low-power applications, including IoT and embedded systems [19]. This study implements a GDI NOR gate, a Half-Adder using PASTA logic, and a

Full-Adder with GDI, demonstrating improvements in energy efficiency, speed, and area utilization, reinforcing GDI-based arithmetic circuits for low-power digital designs.

III RELATED WORK

The Gate Diffusion Input (GDI) methodology has been thoroughly examined as a viable alternative to traditional CMOS logic, especially in the context of low-power VLSI circuit design. Investigations have highlighted the advantages of GDI in minimizing power usage, reducing the number of transistors, and decreasing propagation delays, thereby establishing it as a promising strategy for the development of energy-efficient digital circuits. Research indicates that fundamental logic gates, including NAND, NOR, and XOR, when realized through GDI, utilize fewer transistors and exhibit considerably lower power consumption in comparison to conventional CMOS implementations. In the domain of arithmetic circuits, GDI-based adders have garnered significant attention. Studies have shown that GDI Half-Adders and Full-Adders not only enhance power efficiency but also improve operational speed while ensuring precise arithmetic functionality. Moreover, some research has investigated the combination of GDI logic with asynchronous computing methodologies, such as PASTA logic, to further enhance performance. Circuits based on PASTA logic contribute to increased computational efficiency by minimizing latency, rendering them particularly advantageous for low-power applications. Additionally, numerous studies have employed Cadence Virtuoso for the simulation of GDI-based circuits, assessing their performance through analyses of power, delay, and area. Previous research has validated that GDI logic significantly enhances energy efficiency in arithmetic circuits. This project builds upon earlier findings by implementing a GDI NOR gate, a Half-Adder utilizing PASTA logic, and a Full-Adder designed with GDI, thereby showcasing their benefits in low-power computing scenarios.

IV PROPOSED SYSTEM

In contemporary VLSI design, the imperative to minimize power consumption and transistor count while simultaneously enhancing performance presents a significant challenge. The Gate Diffusion Input (GDI) technique emerges as a viable alternative to traditional CMOS logic, facilitating the creation of low-power, high-speed circuit designs with reduced complexity. This research project is centered on the development of a GDI-based NOR gate and its subsequent integration into a Half-Adder utilizing Priority Asynchronous Spiking Time-dependent Architecture (PASTA) logic. Furthermore, a Full-Adder will be constructed using GDI logic to achieve further performance optimization. The primary objective of this study is to investigate the benefits of GDI technology in the context of arithmetic circuit design, particularly regarding power efficiency, propagation delay, and area reduction in comparison to conventional CMOS implementations. The initial phase of the project entails the design and simulation of a GDI-based NOR gate, which is a crucial element in both arithmetic and logic circuits. This NOR gate will be developed using the GDI technique to achieve reductions in both transistor count and power consumption. The circuit will be simulated using Cadence Virtuoso, where transient and DC analyses will be conducted to assess its performance. Essential parameters such as power dissipation, delay, and area will be extracted and compared with those of a conventional CMOS NOR gate to underscore the advantages of GDI technology.

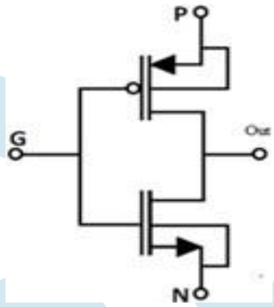

FIG- GDI CELL

In the subsequent phase, a Half-Adder circuit will be designed by integrating GDI NOR logic with PASTA logic. The choice of a PASTA-based asynchronous design is motivated by its potential to decrease latency and improve operational efficiency. The Half-Adder will be realized using optimized GDI-based logic gates, ensuring minimal power dissipation while preserving computational accuracy. Performance metrics, including power consumption, propagation delay, and transistor count, will be analyzed and compared with those of a traditional CMOS Half-Adder, thereby demonstrating the efficacy of combining GDI NOR logic with PASTA principles. This analysis aims to evaluate the efficacy of combining GDI NOR logic with PASTA principles in the context of arithmetic operations. The concluding phase of this study will focus on the development of a Full-Adder circuit utilizing GDI logic. This Full-Adder is intended to enhance the efficiency of sum and carry operations while minimizing power consumption and spatial requirements. Circuit simulation and performance assessment will be conducted using Cadence Virtuoso. A comparative analysis will be performed between the power, delay, and area metrics of the GDI Full-Adder and a traditional Acknowledgment CMOS Full-Adder, highlighting the benefits of GDI-based arithmetic circuits. It is anticipated that the results will reveal substantial enhancements in energy efficiency, positioning GDI Full-Adders as more appropriate for low-power VLSI applications Project is expected to demonstrate that the GDI NOR gate will achieve lower power usage and a decreased transistor count relative to its CMOS equivalent. The Half-Adder designed with PASTA logic and GDI NOR logic is projected to outperform in terms of propagation delay and energy efficiency. Additionally, the GDI-based Full-Adder is expected to offer a more compact and energy-efficient alternative to CMOS Full-Adders, thereby underscoring the advantages of GDI logic in arithmetic operations. The comparative study will substantiate the viability of employing GDI technology for the design of low-power, high-performance digital circuits

V. SIMULATION RESULTS

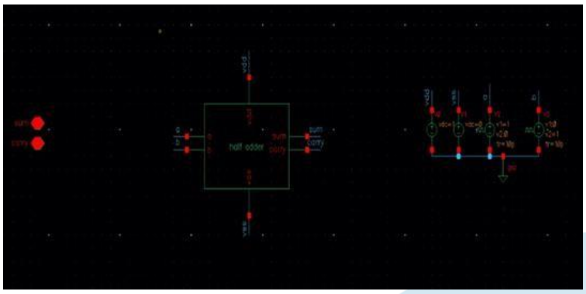

Fig 1

This diagram illustrates a half-adder circuit implemented using CMOS logic gates. It includes XOR and AND gates with their corresponding inputs (A and B), outputs (Sum and Carry), power supply connections (VDD and GND), and a test bench setup for simulation purposes.

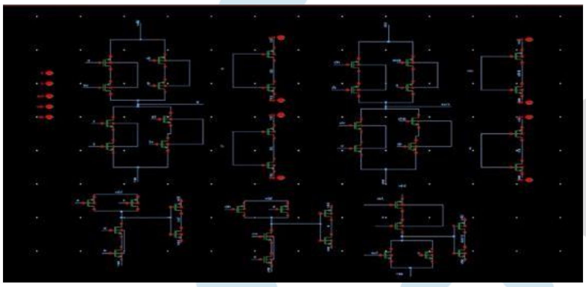

Fig 2

This schematic depicts a full adder circuit implemented using CMOS logic. It illustrates the intricate arrangement of PMOS and NMOS transistors to achieve the sum and carry outputs, demonstrating the fundamental building blocks of digital arithmetic circuits.

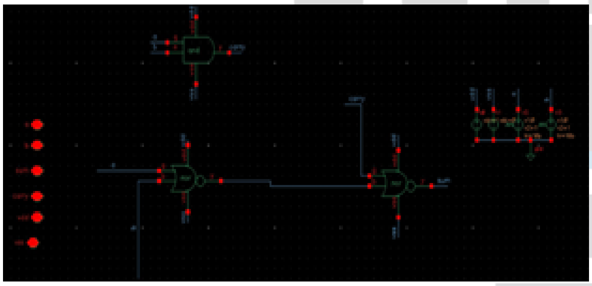

Fig 3

This image illustrates a GDI half-adder implemented using NOR logic. Inputs 'a' and 'b' are fed into an AND gate for the carry output. They also connect to two cascaded NOR gates for the sum. Power (VDD) and ground (VSS) are provided. The GDI structure, indicated by PPA/PDA labels, optimizes transistor usage. The right side shows voltage sources with rise/fall times (tr/tf=10p), simulating the circuit's operation. The design showcases a compact, efficient half-adder using NOR gates within the GDI framework.

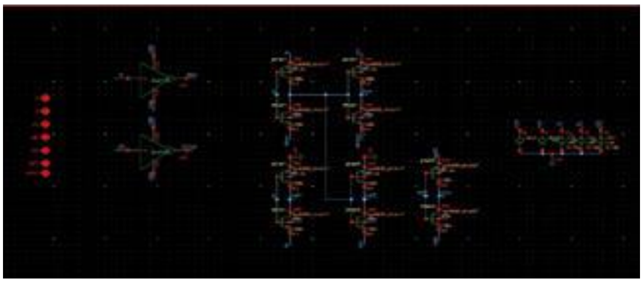

Fig 4

This schematic presents a full adder circuit designed using Gate Diffusion Input (GDI) technology. It showcases the implementation of XOR and multiplexer logic with reduced transistor count, achieving efficient computation of sum and carry outputs. A test bench is included for functional verification.

Fig 5

This transient response graph showcases a GDI full-adder's operation. Inputs A (cyan), B (magenta), and a likely carry-in (implied by the full-adder context) trigger Sum (green) and Carry (red) outputs. The graph illustrates the circuit's timing and functional correctness. The noisy power supply (VO/MINUS) suggests potential issues. The waveform's transitions confirm the full-adder's logic behavior within the Gate Diffusion Input framework.

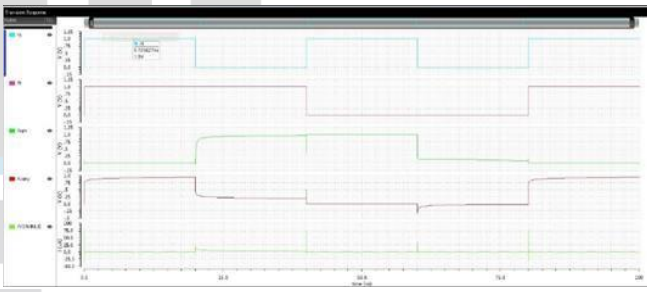

Fig 6

This transient response graph depicts a GDI half-adder using NOR logic. Inputs A (cyan) and B (magenta) drive Sum (green) and Carry (red) outputs. The graph illustrates the circuit's functional behavior over time, showing voltage transitions corresponding to logic states. A noisy power supply (VO/MINUS) is also visible, suggesting potential instability. The graph confirms the half-adder's operation and timing characteristics within the GDI-NOR implementation.

VI TABULATION

TABLE 1 GDI CELL FUNCTION

N	P	G	OUT	FUN
1	B	A	A+B	OR
B	0	A	AB	AND
$\bar{B}$	B	A	$\bar{A}B + \bar{B}A$	XOR
B	$\bar{B}$	A	$AB + \bar{B}\bar{A}$	XNOR
0	$\bar{B}$	$\bar{A}$	$\overline{A+B}$	NOR
$\bar{B}$	1	A	$\overline{AB}$	NAND

This table outlines the versatile functionality of a Gate Diffusion Input (GDI) cell. By varying the N, P, and G inputs, it can realize essential logic functions like OR, AND, XOR, NOR, and NAND. This demonstrates GDI's efficiency in implementing diverse logic operations with a single cell structure.

TABLE 2 POWER CONSUMPTION (unit-watt)

LOGIC GATES	CMOS LOGIC	GDI LOGIC
AND	33.1E-9	1.035E-9
OR	76.81E-9	1.832E-9
NAND	33.01E-9	35.06E-9
NOR	30.41E-9	38.05E-9
XOR	145.6E-9	24.23E-9
XNOR	98.63E-9	35.44E-9
HALF ADDER	13.94E-6	883.6E-9
FULL ADDER	7.702E-6	287.6E-9

This table compares the power consumption of various logic gates (AND, OR, NAND, NOR, XOR, XNOR, Half Adder, Full Adder) implemented using CMOS and GDI logic. The values, expressed in watts (W), highlight the significant power reduction achieved with GDI technology compared to traditional CMOS for most gates.

VII RESULTS

The simulation outcomes obtained from Cadence Virtuoso indicate that the GDI-based circuits present superior performance compared to traditional CMOS designs, particularly in aspects of power consumption, transistor utilization, and propagation delay. The GDI NOR gate shows a marked reduction in power dissipation and an increase in switching speed relative to its CMOS equivalent. Furthermore, the Half-Adder, which employs GDI NOR logic in conjunction with PASTA logic, demonstrates enhanced computational efficiency and lower latency. This configuration utilizes a smaller number of transistors while ensuring precise sum and carry outputs. Additionally, the Full-Adder constructed with GDI logic achieves diminished power consumption, simplified circuit architecture, and minimal propagation delay. Collectively, these findings substantiate the assertion that GDI-based circuits significantly improve energy efficiency and performance, rendering them particularly advantageous for low-power VLSI applications.

VIII CONCLUSION AND FUTURE SCOPE

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