Implementation of low power full adder using CMOS technology

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***Abstract*---A crucial part of digital and VLSI systems is played by adders. The use of arithmetic operations is crucial in digital systems. The entire study in VLSI systems is focused on reducing the transistor scale to enforce any other digital system. This suggested design is implemented by various logic system types, each of which plays a specific function in the hybrid system. This structure uses a hybrid Full Adder cell with a single bit. Using a 16-nm CMOS hybrid full adder, the proposed approach is studied. Based on the findings of the simulation, the suggested architecture shows significant efficiency in both power consumption and delay. The simulation's output indicated that the data channel architecture for contemporary high speed central processor units used a full adder circuit. This type of hybrid full adder, which is mostly employed in nanotechnology applications, decreases latency while enhancing efficiency. For a 1 -V supply at 16-nm technology, the average power consumption of 1.5317µW with moderately low delay of 10.4078n was determined to be incredibly low. Compared to earlier full adder designs, this form of adder offers considerable advantages in power, high speed.**

***Index Terms*—efficiency, power, delay, high speed**

I. INTRODUCTION

Today's technology reduces gate length and transistor thickness as it moves from micrometer to nanoscale scale. Full adders are crucial to VLSI systems because they boost the efficiency of digital and nano computing systems. Minimizing power consumption for digital systems requires optimization at all design stages.

This paper illustrates the approach of creation that incorporates the technologies for creating digital circuits, their architectural designs, and the most advanced algorithms. Arithmetic units are employed in contemporary computing applications to increase the effectiveness of adder systems. The hybrid adders highlight the significance of low power design approaches. In this transistor logic, the transistors serve as voltage-controlled switches. A complete adder is employed with various logic models and offers various advantages. As a result, these various complete adder types can implement the methods in microprocessor systems.

The logic design style of Hybrid-CMOS uses more than one element full adder design. For example, this kind of adders added in to the hybrid CMOS design. The different method of adders are use more than one logic design, called as hybrid-logic design style, these hybrid full adder designs is used for complex circuits and it's also used in nano technology applications. This style of logic design gives the high efficiency and high performance of logic circuits. The one bit full adder performance is good but the performance degenerated rustically as the chain size increased. A new 1 bit hybrid full adder using different types of gates like PTs ,TGs, and static CMOS logic was introduced. In this type of hybrid full adder was designed by 16 nm technology. To comparing C-CMOS circuits, the hybrid structure circuit gives high speed, low power.

II. WORKING FUNCTIONALITY

This technique made use of PTs, TGs, and C-CMOS circuitry, creating a hybrid FA. The hybrid adder circuit's primary capacity is one of its most valuable resources, and researchers are working to preserve this form of reasoning.

This study illustrates the switching behavior, transistor size, and intermediate node capacitances as the power dissipation characteristics in CMOS circuits (diffusion, gate and wiring capacities). A recent technique for analyzing the behavior of hybrid logic circuits has been developed in order to prevent complicated structure.

The major goal of this study is to apply several types of logic styles to enhance the hybrid structure. In instance, while using a typical tool, a large delay error and excessive power usage occur. Use the Spice tool, which uses smaller transistors and lower power and delay requirements, to prevent this kind of error.

It is possible to improve the time analysis of nanotechnologies by using hybrid structure methodologies. Currently, researchers are utilizing a hybrid design method that combines the advantages of many logic types into a single full adder unit. TG Adder (TGA) and Transmission Function Adder are used to utilize TGs in the architecture (TFA). The key advantage of TGA and TFA FA is that they do not experience voltage loss or poor performance.

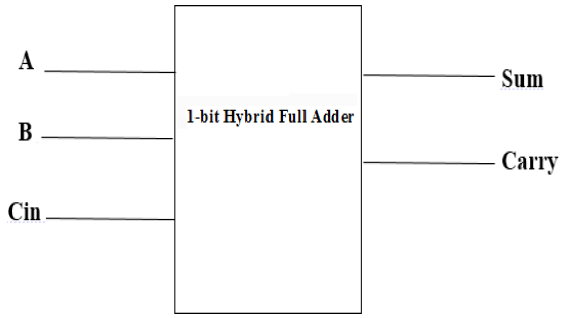

Figure 1: Symbol diagram for one bit Hybrid full adder

The hybrid full adder has two types of combination there are static and dynamic. The main focus of hybrid logic adder search includes different types of adder based on separate types of logic designs is expressed. This kind of adders are basically used in nano technology implementation in recent circuit

PROPOSED FULL ADDER DESIGN

In this study, a hybrid full adder architecture with a single bit implementation is developed. Its hybrid structure provides low power consumption, high speed, and excellent efficiency when compared to earlier traditional adders. The suggested system's main design is based on 16 nm technology.

Hybrid-CMOS Logic Design

The following phrases represent the carry and sum generation components of the hybrid FA architecture. The primary accomplishment of VLSI design circuits is to decrease transistor size while increasing high speed and using less power. With a 0.8V power supply and 22nm CMOS technology, the suggested technique shows reduced size. The following block diagram shows the fundamental block diagram

for the suggested method.

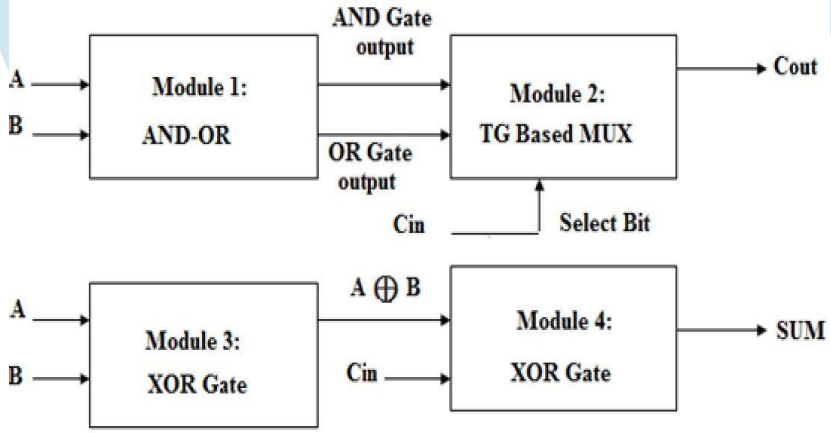

Figure2:Proposed Fulladder Block Diagram

In this study, a new hybrid FA with various transistor logic designs has been proposed as the system. The 16 nm technology was used to execute the suggested complete adder design. A comparison of the design's output parameters with 20 other FA designs with power supplies ranging from 0.4 V to 1.2 V was done to ascertain the design's reliability.

The existing full adder demonstrated performance in various power supply ranges when compared to the existing FAs. The following circuit diagram shows the carry and sum generation. The suggested method is put into practice utilizing CMOS technology, which decreases latency, and is particularly useful for low power design circuits. 16nm technology was used to construct the suggested complete adder. By lowering the supply voltage by 1 volts, the digital circuits efficiency is increased.

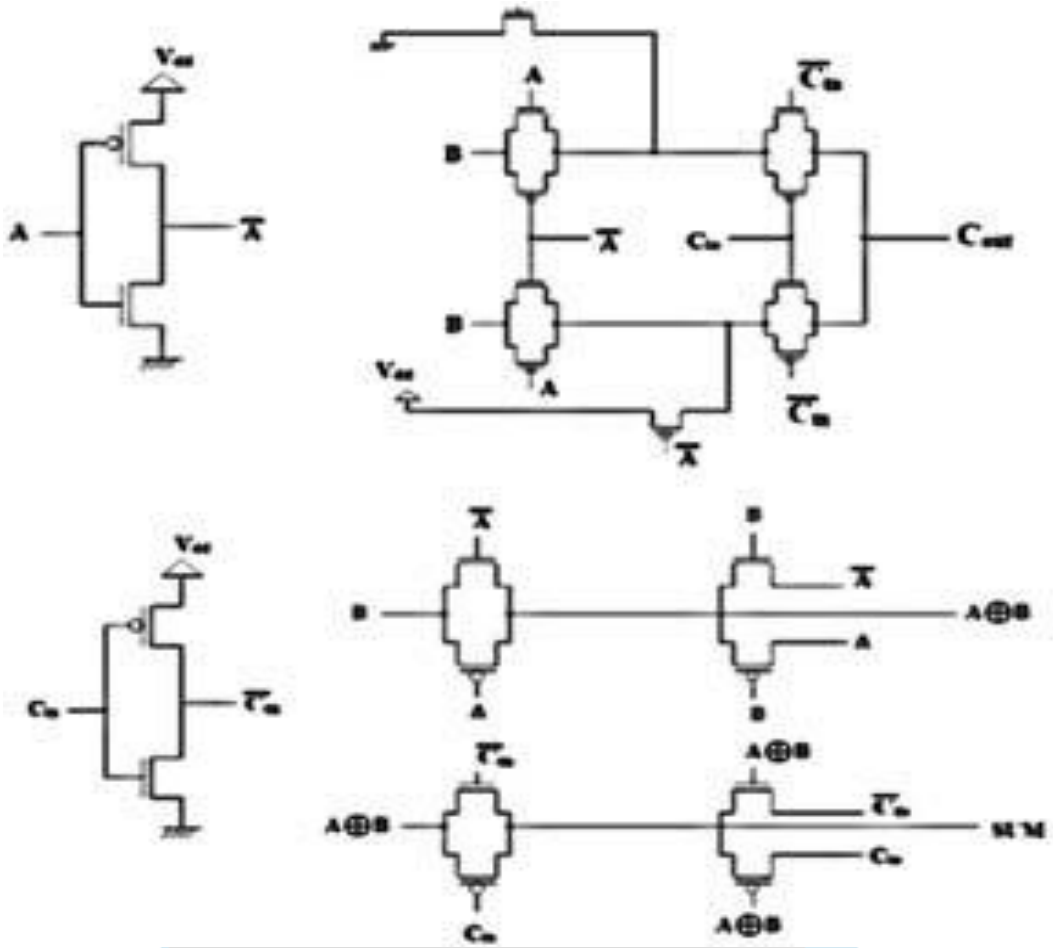

Figure3:Proposed Full Adder Carry and Sum Generation

III. SIMULATION AND RESULTS

In this CMOS technology simulation, 16 nm was used to simulate various performance metrics. The suggested system's results demonstrate that the FA improved simulation outcomes at a supply voltage of 1V. The suggested hybrid full adder's results demonstrate that the power and delay products are more efficient. The picture below shows the input and output simulation.

PROPOSED DESIGN

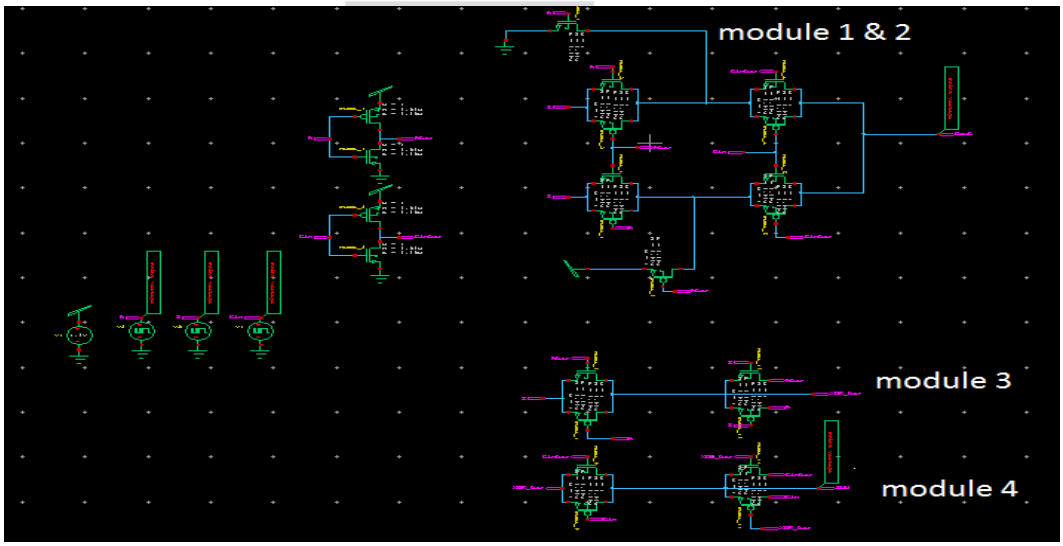

Figure 4: Circuit design of one bit hybrid full adder

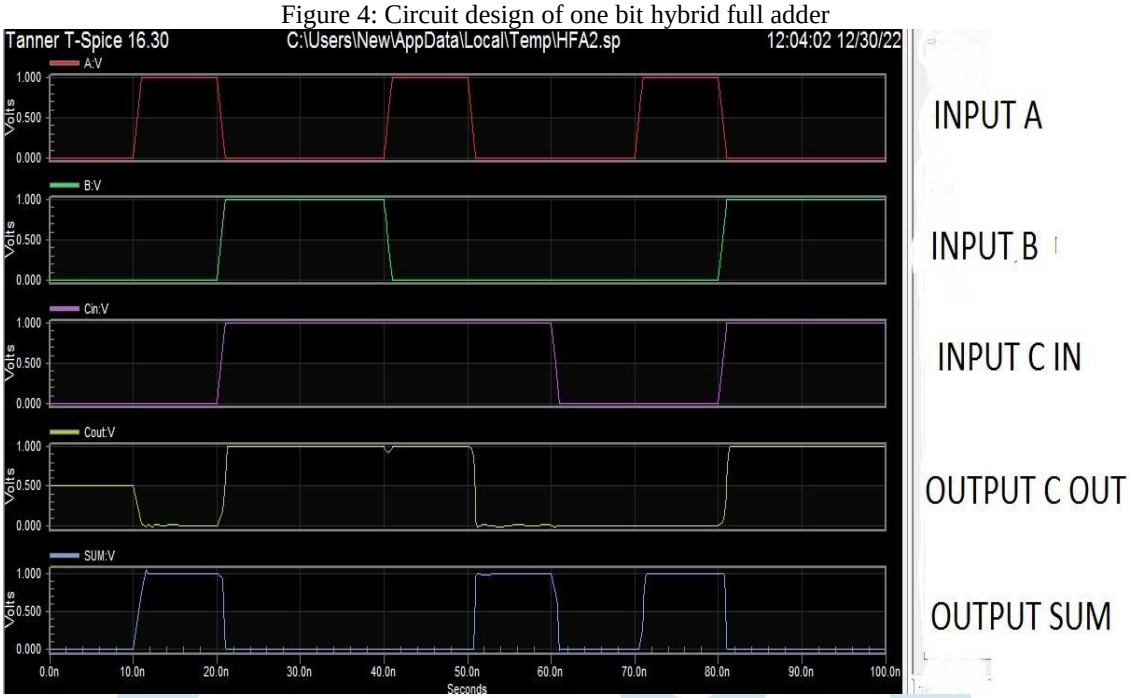

Figure 5: Simulation results for the one bit Hybrid fulladder

The design of proposed system does not achieve the best power efficiency, the value is still small enough in modern processors for practical use. The proposed fulladder will work is 16 nm technology with a minimum supply voltage of 1V.

IV. Power and delay Analysis

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Power Results

VV1 from time 0 to 1e-007
Average power consumed -> 1.531773e-007 watts
Max power 4.046974e-005 at time 5.0875e-008
Min power 6.609388e-009 at time 3.5e-009

VV2 from time 0 to 1e-007
Average power consumed -> 2.240892e-007 watts
Max power 2.580111e-005 at time 7.09375e-008
Min power 0.000000e+000 at time 0

VV3 from time 0 to 1e-007
Average power consumed -> 1.367716e-007 watts
Max power 3.042491e-005 at time 8.1e-008
Min power 0.000000e+000 at time 0

VV4 from time 0 to 1e-007
Average power consumed -> 5.538052e-008 watts
Max power 2.811885e-005 at time 5.09375e-008
Min power 0.000000e+000 at time 0
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Figure6:Simulation result for power analysis

The 1-V supply was found to be extremely low at 16-nm technology, the average power consumption was1.5317µW with a moderately low delay of 7.0415ps resulting in the following figures.

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Measurement result summary
   tdelay               =    10.4078n


Parsing                                0.93 seconds
Setup                                  0.55 seconds
DC operating point                     0.12 seconds
Transient Analysis                     0.59 seconds
Overhead                               3.17 seconds
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Total                                  5.35 seconds
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Figure7: Simulation result for power analysis

V. CONCLUSION

A one-bit hybrid full adder with low power consumption, little latency, and good performance has been implemented. Comparing the proposed design's features against those of existing FAs. The hybrid circuits are created using several logic approaches. The proposed Full Adder shows improved speed and power performance and can be used to implement circuits with minimal power requirements. Using a 1-V supply, a power consumption of 1.5317µW was discovered for 16-nm technology. Both CMOS and nanotechnology-based VLSI circuits and systems can use the suggested adder. Performance of this suggested method was applied to circuits with lower power requirements used in nanotechnology applications. Moreover, hybrid design logic circuits are primarily employed to create design circuits with low power consumption, and high efficiency.

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