Power Efficient Precharge Free 6-T Content Addressable Memory

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***Abstract*: Recent advancements made in the field of electronics over last few decades lead to unique challenges in system design. The compact device sizes and their capability to process complex inputs at a faster rate attracted many applications. The conventional mechanical systems are being replaced by either electromechanical systems or electronic systems in automotive industry, smart homes, and portable devices etc. Memory will always be integral part of any electronic processing system design. Improvements of memory technology improves overall efficiency generally. Out of many different memories designed from different devices, semiconductor MOS memory is most widely used today. Conventional memories such as Random Access Memory(RAM) or Read Only Memory(ROM) requires more time to search a particular word of data is present or not. Hence Content Addressable Memory (CAM) are designed for fast and parallel searches. This paper reviews different types of such CAM cells based on features. New power efficient pre-charge free CAM is proposed. The performance is compared by simulation in 45nm technology. There is a considerable reduction in power consumption and delay is reduced at the cost of additional transistor.**

***keywords*: Content Addressable Memory (CAM), MOS, SRAM**

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1. INTRODUCTION

A memory is an integral part of any electronic system design to store data. Various types such as Random Access Memory (RAM), Read Only Memory (ROM) etc. are available suitable for different system designs. Content Addressable Memory (CAM) is a type of memory which stores data along with the capability of matching operations. Many different applications of real world today requires parallel fast search and matching of data. The comparison is between data to be searched and data stored in memory. If they both are equal, an output line indicates match. Similarly, when they both are unequal, negated value of the output line indicates mismatch. Data can be searched in a large chunk of memory simultaneously. The search process is completed within a single clock cycle. Match evaluation output line can be used as control input processing system after match of a particular data in memory array. Lower power consumption and faster match line evaluation of CAM attracts many advanced applications.

Currently many electronic devices are developed to be battery operated. Drastic increase in battery operated devices coupled with technology scaling lead to many different challenges in system design. With the rise of scale of integration, small sized high density chips developed have high probability of suffering from instability. Similarly, the existing CAM cells may not be able to perform up to the needed requirements. Hence there exists a need to come up with different CAM cells for different system designs, which may be optimized in terms of any of parameters such as area, power, delay etc. Always there exists a trade-off between different parameters. Fulfilling all parameter optimization in a single CAM cell is highly impossible. Based on requirements for specific application, certain parameter optimized cell can be chosen. This paper describes 8 different types of CAM cells with different number of transistors. The benefits and drawbacks of are also discussed. Later a new CAM cell optimized in terms of power is proposed.

2. METHODOLOGY

The CAM cell consists of two blocks, storage and evaluation. Storage block contains data to be stored in memory and evaluation block evaluates match between search line and stored data. The existing CAM cells are reviewed and new CAM cell is proposed.

2.1 4T XOR CAM

The 4T XOR CAM cell [1] consists of 4 MOSFETs. Fig.1 shows the 4T XOR CAM cell schematic. Transistors connected to word lines are utilized to write the data and other two are used for storing along with evaluation. Asserting high value on word line for write and low for hold. Bit lines act as search lines when word line is low.

This cell design is and reduced area consumption. It can be scaled to high density chips. When used in NOR type CAM array design, fast discharge and improved performance

When used in design of a NOR type CAM array, increase in drain capacitance and hence power consumption

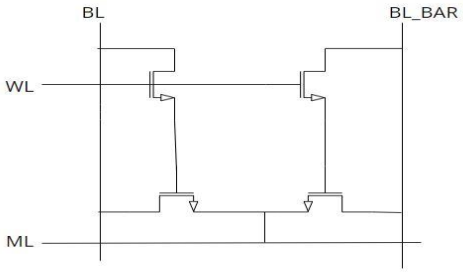

Fig.1 4-T XOR CAM

2.2 6T CAM

The 6T CAM cell [2] consists of 6 Transistors with asymmetric 4T storage cell coupled with NAND compare unit of 2 transistors as shown in Fig.2. Unlike the previous CAM cell it makes use of 2 PMOS in its design.

It is designed using lesser number of transistors as well area utilization is decreased. Suitable for NAND compare circuit. High noise margin for logic 1 storage.

Rise in off chip voltage for inactive word lines increases power consumption substantially. Stability of logic 0 depends on word line bias.

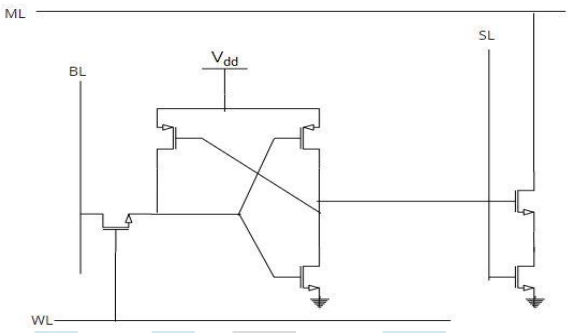

Fig.2 6-T CAM

2.3 7T CAM

Fig.3 shows another CAM cell [3]. It consists of cross coupled PMOS pair for storage of data along with XOR based logic for match line evaluation.

Faster discharge of match lines compared to NAND and NOR based designs. Reduction in area and power with improved performance.

During mismatch it doesn't provide strong 1, pull down transistor is partially ON. Increase in delay due to partially ON transistor.

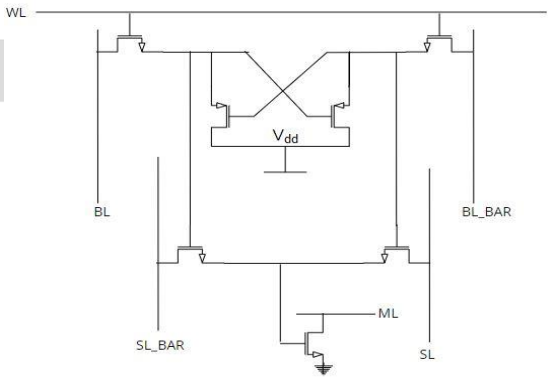

Fig.3 7-T CAM

2.4 8T CAM

Fig.4 shows a 8T SRAM cell [4]. It has cross coupled PMOS pair for storage of data and a unique evaluation logic. It is designed using lesser number of transistors as well area utilization is decreased. Suitable for NAND compare circuit. High noise margin for logic 1 storage.

It is self-controlled and pre-charge free CAM cell. Higher frequency of operation and higher performance. Elimination of dependency of previous ML. Improved operation speed even for larger word lengths.

Increase in area and number of transistors compared to previous CAM cells.

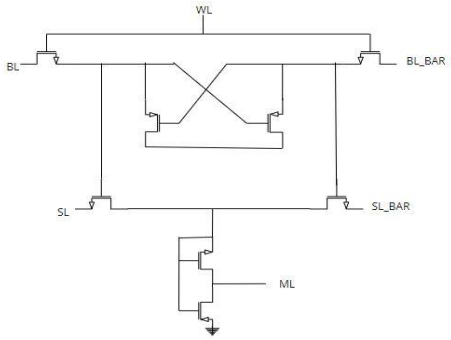

Fig.4 8-T CAM

2.5 9T CAM

The 9T CAM cell[3] shown in Fig.5 is same as 7T CAM cell but makes use of XNOR logic for match line evaluation with an addition of an inverter for control input of match line discharge transistor.

It provides strong 1 during mismatch with the help of additional inverter. Reduction in match line evaluation delay. Higher reliability

Increase in number of transistors compared to previous CAM cells and hence increased area.

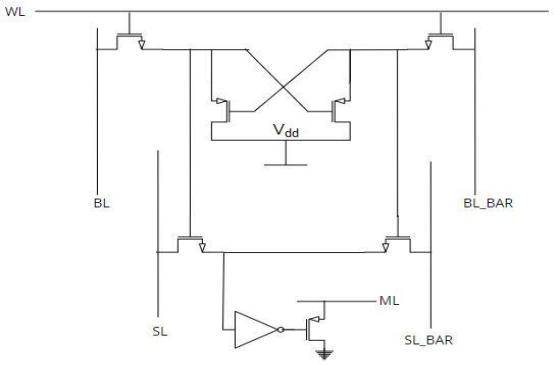

Fig.5 9-T CAM

2.6 10T CAM

Fig.6 shows another CAM cell [4] consisting of 10 Transistors. It is same as 8T CAM cell, but it uses cross coupled inverters to store data instead of cross coupled PMOS pair. The unique evaluation logic is same for both CAM cells.

It is self-controlled and pre-charge free CAM cell. Higher frequency of operation and higher performance. Elimination of dependency of previous ML. Improved operation speed even for larger word lengths.

Increase in number of transistors compared to previous CAM cells and hence increased area.

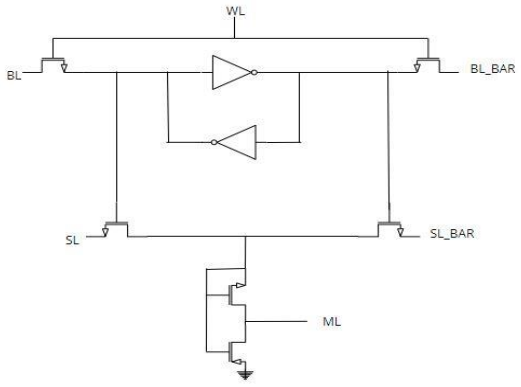

Fig.6 10-T CAM

2.7 11T CAM

Fig.7 shows 11T CAM cell [5]. It has 6T SRAM for storage unit with addition of a transistor for a NOR type CAM using 10-T which is most often in conventional applications.

Considerable saving of leakage current during standby mode due to stacking effect from additional transistor.

Increase in area and number of transistors compared to previous CAM cells.

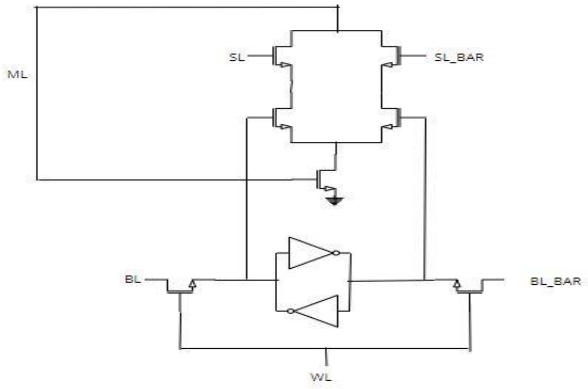

Fig.7 11T CAM

2.8 12T CAM

Fig.8 shows 12T CAM cell [5]. It has similar structure as that of 11T CAM along with an extra PMOS transistor for power supply of inverters of 6T SRAM.

Reduction in dynamic power consumption. Reduced leakage power.

Rise in area and number of transistors.

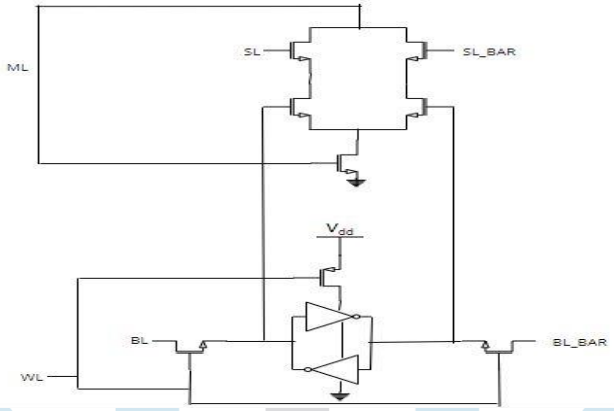

Fig.8 12-T CAM

3. POWER EFFICIENT PRECHARGE FREE CAM

Conventional CAM cells should be capable of basic operations – write, pre-charge and evaluate. Pre-charge phase hinders the speed of operation of match evaluation. A new CAM cell is proposed in this paper that consists of minimum number of transistors for storage unit (only 4) and pre-charge free evaluation logic. The speed of operation is significantly improved compared to CAM cells with pre-charge phase. The bit lines itself act as search lines and data to be searched is sent on bit lines when storage unit is in standby mode. The evaluation logic consists of a CMOS network, with PMOS connected to ground and NMOS connected to XNOR operation of stored data and data to be searched. The proposed 6-T CAM is shown in Fig.9

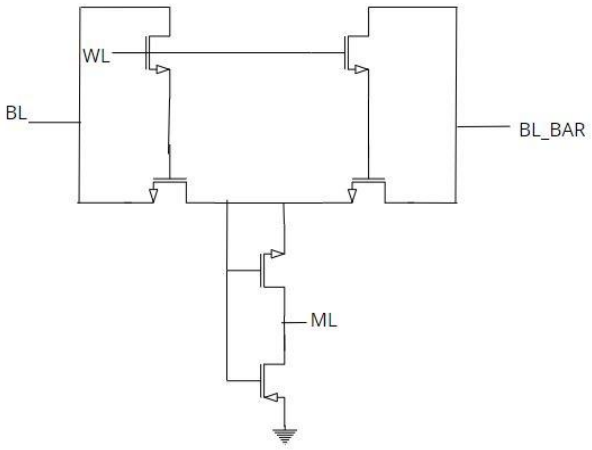

Fig.9 Pre-charge Free 6-T CAM

4. RESULTS

The proposed CAM cell is simulated in 45 nm technology using Cadence Virtuoso tool. The Evaluation delay and power consumption are measured and compared with existing CAM cell as shown in Table 1. The simulation results show that proposed CAM cell has marginally better delay and significant reduction in power consumption.

5. Table 1: Existing vs Proposed CAM Comparison

CAM Cell	Transistor Count	Delay(ns)	Power(nW)
Existing	5	2.11	0.9218
Proposed	6	1.97	0.4108

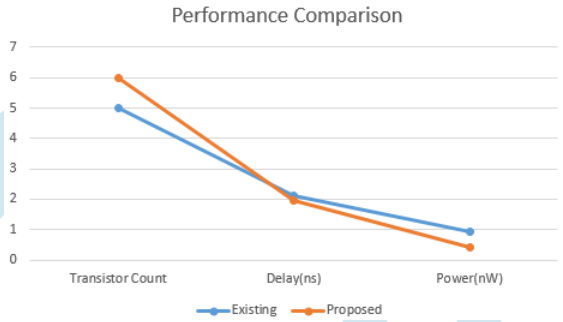

Fig.10 : Performance Comparison Existing vs Proposed CAM

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