Design of 16-bit ALU Using Full-Swing GDI Technique

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***Abstract*—The Arithmetic Logic Unit is an integral part of the central processing unit of a computer. It carries out basic arithmetic operations like addition, subtraction, increment, decrement, etc. as well as logic operations like AND, OR, XOR, etc. The ALU is realized with transistor circuits. The overall power consumption of the device increases as the CPU power increases. Power dissipation is a crucial factor in low power VLSI circuit designs. The aim of low power VLSI is to minimize the power of individual components, which in turn decreases the overall power consumption. In this work, a 16-bit ALU is designed using Full-Swing GDI technique, which is an effective method of power and area reduction. From the simulation results we conclude that the ALU designed using FS-GDI technique consumes less power, while giving full swing output. The simulations are run in Cadence Virtuoso, 45nm Technology.**

***Index Terms*—ALU, FS-GDI, m-GDI, low power.**

I. Introduction

Very Large-Scale Integration makes it possible to integrate around 1 million transistors on a single chip. In the past, the primary concern of VLSI chips was area, cost, reliability and performance. Power was given secondary importance. This trend has changed and now power is given first importance than the speed and area. Nowadays there is a rising demand for portable devices and longer battery life. Thus, power consumption is becoming a crucial factor for designing VLSI circuits. The arithmetic logic unit forma a fundamental part of the brain of the computer. The ALU's power consumption has a direct impact on processor's power dissipation [8]. This paper presents a 16-bit ALU which consists of multiplexer, adder and logic block. Full-Swing GDI, a design method that uses less transistors than CMOS and produces full swing output as compared to modified GDI (m-GDI), is used to design the components.

II. Design Techniques

CMOS Technique

CMOS is an abbreviation for a Complementary Metal Oxide semiconductor. It incorporates both NMOS and PMOS transistors. The pull-up network constitutes of PMOS transistors while the pull- down network constitutes of NMOS transistors. Prior to CMOS, PMOS and NMOS were used individually in electronic devices. Among these, NMOS became more widely used due to its fast operation and low cost compared to PMOS. NMOS has its own disadvantages such as more static power consumption. When NMOS and PMOS are used together in a single IC symmetrically, it provides flexibility in circuit design. CMOS also has the advantage of low power consumption, it consumes almost zero power during static conditions. The advantages of CMOS logic are transistor sizing, robustness and reliable operation at low speed [4]. Figure 1 shows the basic CMOS cell.

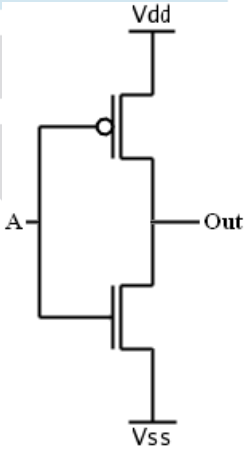


Figure 1: Basic CMOS cell

GDI and m-GDI Technique

GDI stands for Gate Diffusion Input. This design technique is used for reducing power in circuits. Along with power it also reduces the area of the circuit. The various logic functions such as AND, OR, etc. can be realized using only two transistors, one

PMOS and one NMOS. The logic operations that can be implemented using a basic GDI cell are listed in the Table I. Fig 2 shows the basic GDI cell.

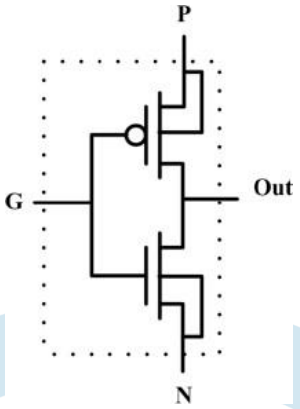


Figure 2: Basic GDI cell

Table 1 Logic functions realized using basic GDI cell

N	P	G	OUT	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B$+AC	MUX
0	1	A	$\overline{A}$	NOT

Modified GDI or m-GDI technique is adopted from GDI technique. In this, all the body terminals are maintained at the same potential i.e. body of all PMOS and NMOS are wired to V_{DD} and V_{SS} appropriately.

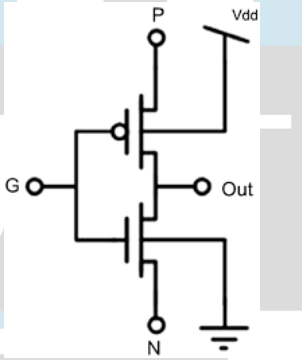


Figure 3: Basic m-GDI cell

The drawback of GDI and m-GDI technique is that it is not possible to achieve full swing output voltage.

FS-GDI Technique

FS-GDI stands for Full Swing Gate Diffusion Input. It is an efficient low power design technique that reduces delay and power consumption. Full swing GDI technology offers faster operation than CMOS technology [3]. Although this technology employs more transistors than the m-GDI technique, it still requires fewer transistors than the CMOS technique. It is a technique derived from m-GDI technique which is used to enhance the output swing. To get full swing output, it is utilised as an alternative to swing restoration buffers [4].

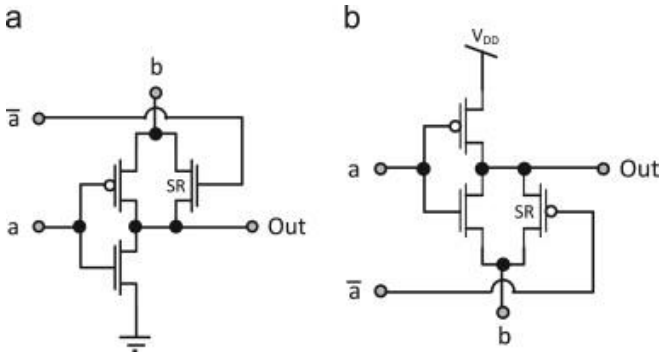


Figure 4: Basic FS-GDI cells

III. PROPOSED 16-BIT ALU

Inverter

Inverter (NOT gate) is a logic gate which performs negation operation. The following schematic shows inverter schematic used in the ALU design. A symbol is created for the schematic shown below.

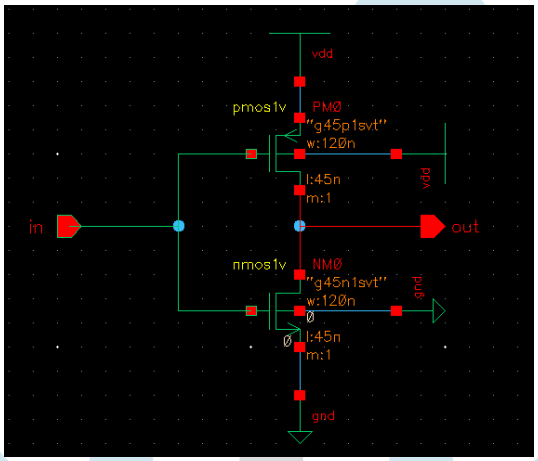


Figure 5: FS-GDI Inverter (NOT gate)

Multiplexer

Multiplexer (MUX) is also called a data selector. The device chooses among the available inputs based on the input at the select line. Two inputs, one output, and one select line make up a 2:1 MUX. Four inputs, one output, and two select lines make up a 4:1 MUX. Three 2:1 MUX combines to form a 4:1 MUX. The following schematics show a 2:1 MUX in FS-GDI and a 4:1 MUX using the FS-GDI 2:1 MUX. Symbols are created for these schematics.

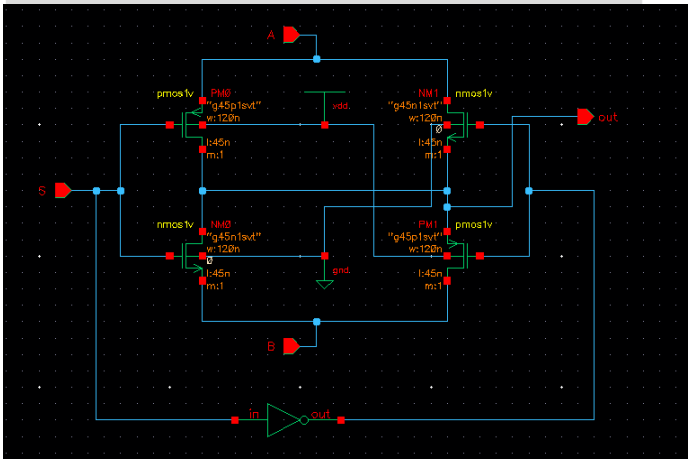


Figure 6: FS-GDI 2:1 MUX

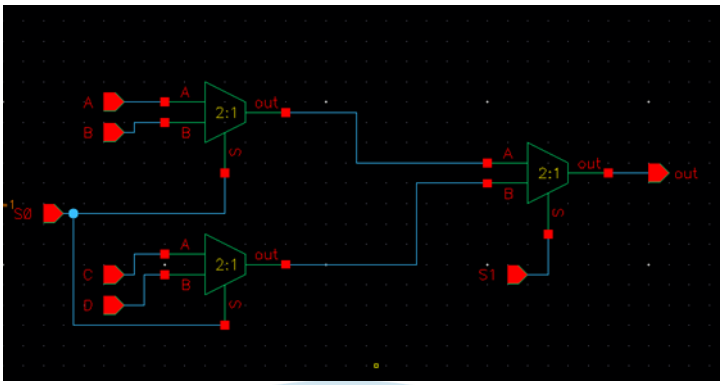


Figure 7: FS-GDI 4:1 MUX

Full Adder

Full adder is a combinational circuit that arithmetically adds the three input bits [3]. This adder is designed in FS-GDI using two XOR gates and a 2:1 MUX. The schematic of the full adder is shown. A symbol is created for the schematic shown.

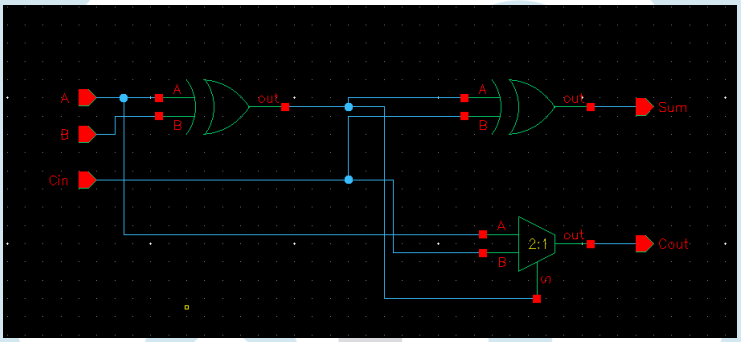


Figure 8: FS-GDI Full Adder

EXOR Gate

EXOR gate is a logic gate that gives a true or high output only when the inputs provided are complement of each other. If both inputs of the gate are same (either high or low) then the output is false or low. This gate is used in full adder to obtain the sum output. It is also used in the logic block of the ALU. The schematic of XOR gate is shown. A symbol is created for the schematic shown.

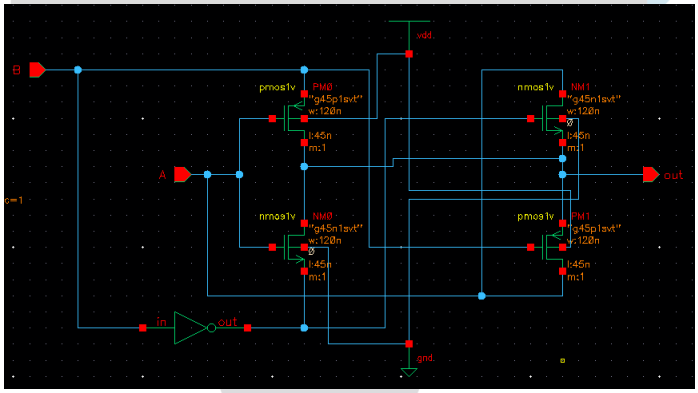


Figure 9: FS-GDI EXOR Gate

AND Gate

AND gate is a logic gate that gives a true or high output only when all the inputs provided are high or true. If both or either of the inputs of the gate is low then the output is false or low. The schematic of AND gate is shown. A symbol is created for the schematic shown.

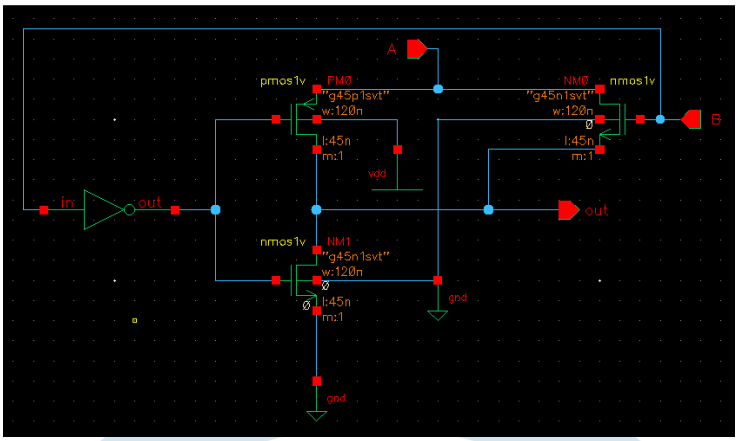


Figure 10: FS-GDI AND Gate

OR Gate

OR gate is a logic gate that gives a false or low output only when all the inputs provided are low. If both or either of the inputs of the gate is high then the output is high. The schematic of OR gate is shown. A symbol is created for the schematic shown.

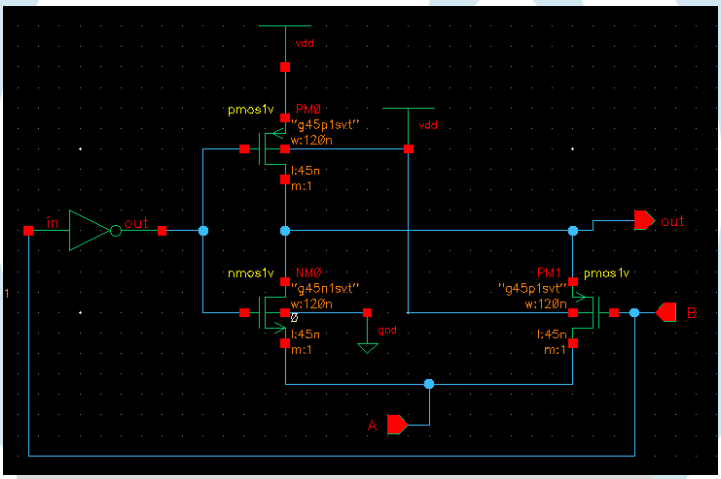


Figure 11: FS-GDI OR Gate

Logic Block

This logic block consists of AND, XOR, XNOR and OR gates. This block is a part of the ALU which performs the logic functions. The schematic is shown below. A symbol is created for the schematic.

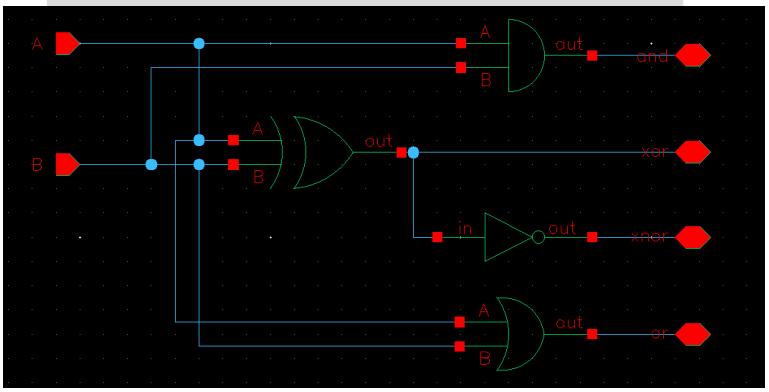


Figure 12: FS-GDI Logic Block

1-Bit ALU

The schematic of the 1-bit ALU implemented [4] is shown below in Fig. 13, it includes a full adder, logic block, 2:1 MUX, two 4:1 MUX and an inverter.

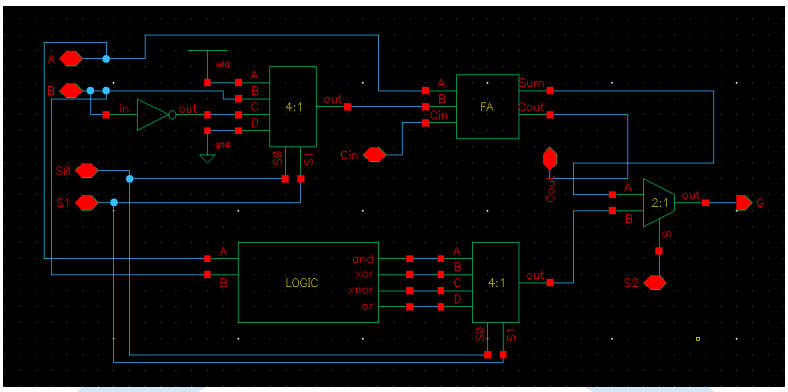


Figure 13: FS-GDI 1-Bit ALU

Table 2 Function table of the ALU

S2	S1	S0	Operations	Function
0	0	0	G = A - 1	DECREMENT
0	0	1	G = A + B	ADDITION
0	1	0	$G = A + \overline{B} + 1$	SUBTRACTION
0	1	1	G = A + 1	INCREMENT
1	0	0	G = A ∧ B	AND
1	0	1	G = A ⊕ B	XOR
1	1	0	$G = \overline{A}$	XNOR
1	1	1	G = A ∨ B	OR

The initial 4:1 MUX and full adder form a part of the arithmetic unit of the ALU. This MUX selects the B operand for the full adder based on the select lines S_1 and S_0. The full adder computes the sum of three bits A, B and C_{in}. The logic block and second 4:1 MUX forms a part of logic unit of the ALU. Based on the select line S2, the 2:1 MUX will choose between the arithmetic unit and the logic unit. The truth table shown in Table II above shows the arithmetic and logic operations performed by the designed ALU.

4-Bit ALU

The schematic of the 4-bit ALU implemented [4] is shown below in Fig. 14, it consists of four blocks of 1-bit ALU and one 2:1 MUX.

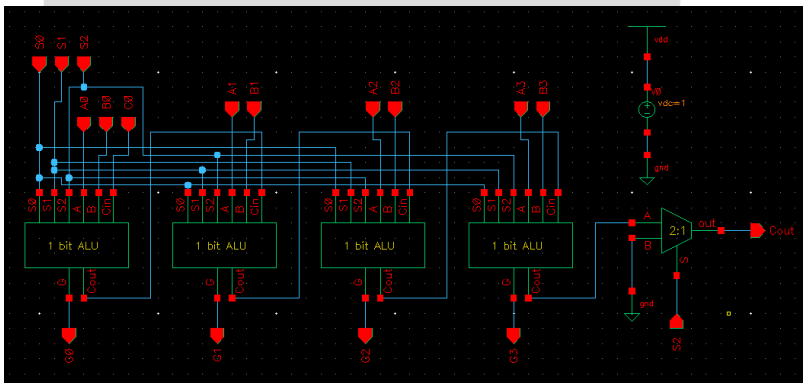


Figure 14: FS-GDI 4-Bit ALU

8-Bit ALU

The schematic of the 8-bit ALU implemented is shown below in Fig. 15, it consists of two blocks of 4-bit ALU and one 2:1 MUX.

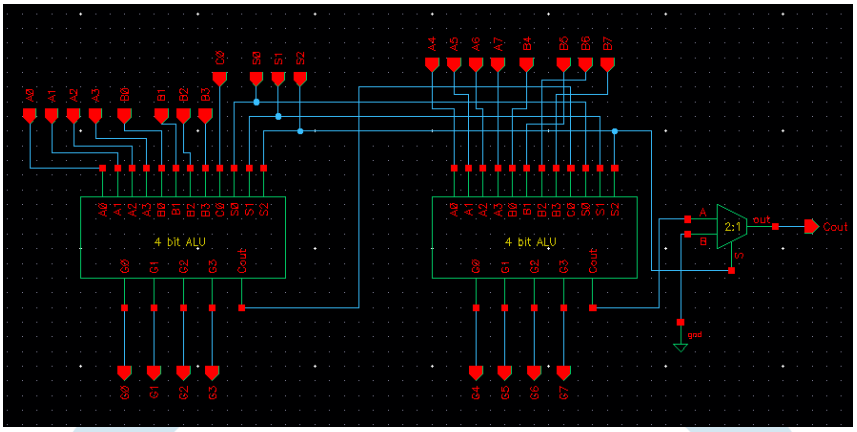
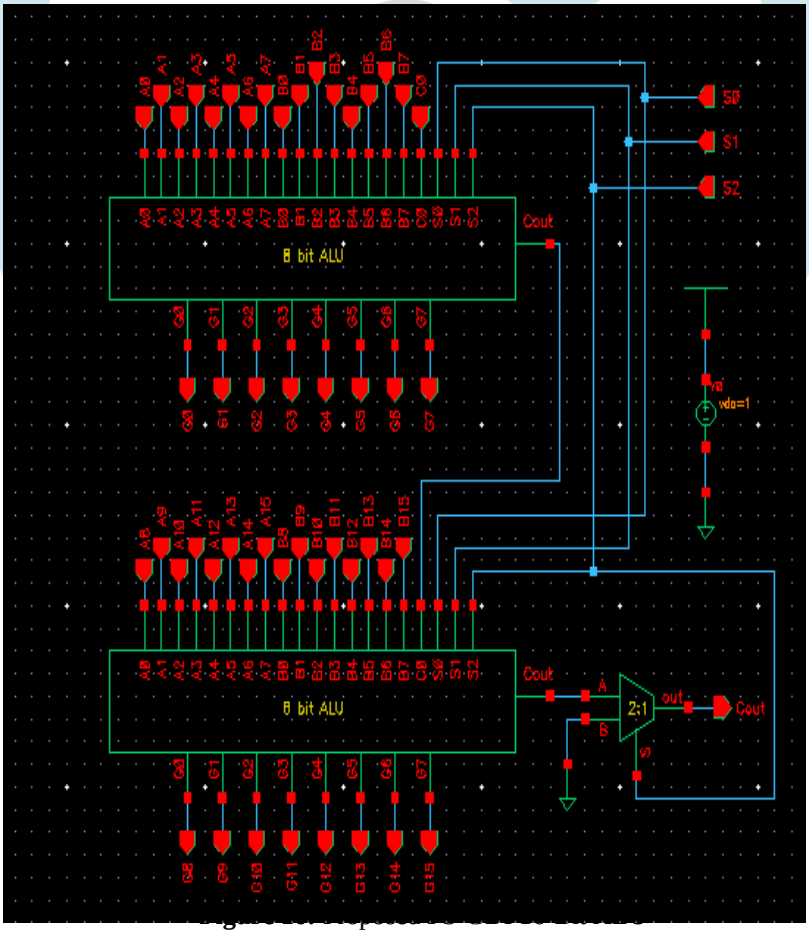


Figure 15: FS-GDI 8-Bit ALU

16-Bit ALU

The schematic of the proposed 16-bit ALU is shown below in Fig. 16, it consists of two blocks of 8-bit ALU and one 2:1 MUX.



IV. SIMULATION RESULTS

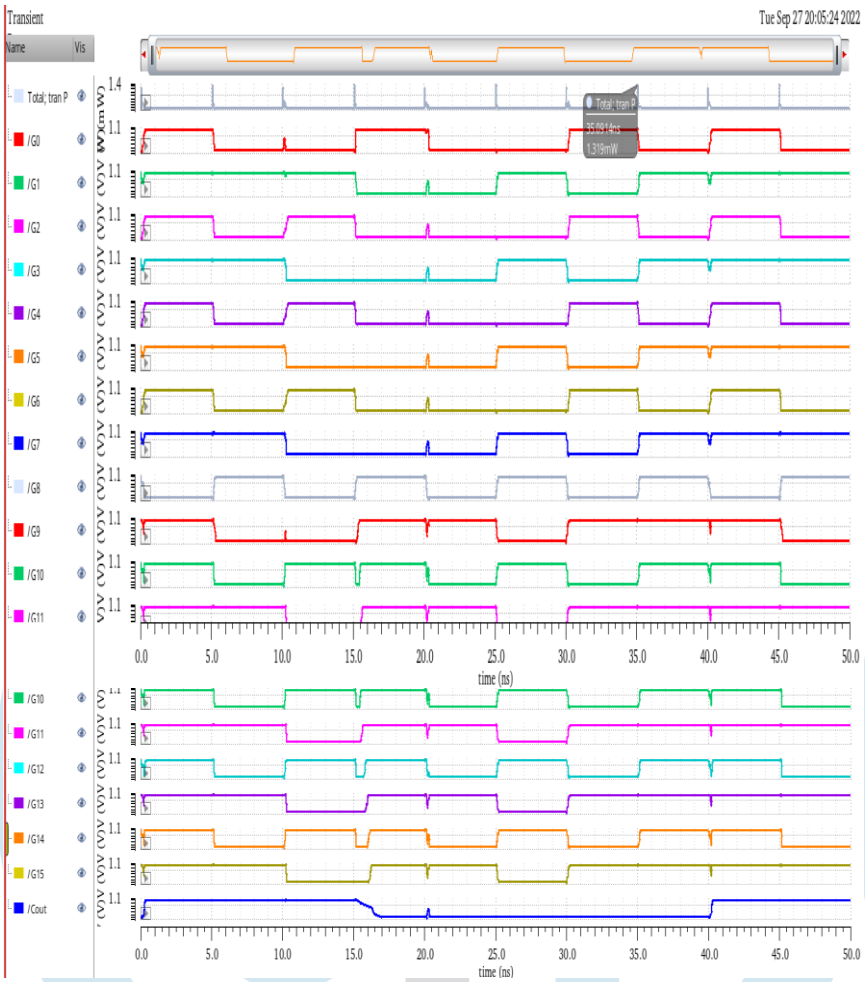


Figure 17: Simulation Graph of Proposed FS-GDI 16-Bit ALU

The proposed 16-bit ALU is designed using Full-Swing GDI Technique. The simulations are performed using Cadence Virtuoso, 45nm Technology, with a power supply of 1V. Fig. 17 shows the simulation graph for the test inputs of A=1111111100000000 and B=1010101010101010. The output graphs are shown for G [15:0] and C_{out}. The transient power wave is also plotted.

Table 3 below compares the power consumption of 16-bit ALUs using various low power design methodologies.

Table 3 Power Consumption Table

Design Technique	Power
CMOS [6]	10.768 W
m-GDI [6]	17.835 W
FS-GDI (this work)	1.319 mW

Table 4 Number of Transistors Comparison

Component	Number of Transistors		
	CMOS	m-GDI	FS-GDI
Inverter	2	2	2
AND gate	6	2	5
OR gate	6	2	5
EXOR gate	22	3	6
2:1 MUX	12	2	6
4:1 MUX	36	6	18
Full Adder	56	8	18
XNOR gate	20	5	8
1-Bit ALU	196	36	86
4-Bit ALU	796	146	350
8-Bit ALU	1604	294	706
16-Bit ALU	3220	590	1418

V. CONCLUSION

This paper presents a 16-bit ALU which is designed using a low power technique, Full-Swing Gate Diffusion Input. It consists of 1418 transistors totally and has a transient power of 1.319 mW. The simulations are performed in Cadence Virtuoso, 45nm Technology with a supply of 1V. The results obtained are tabulated. The results show that this work has less transient power and produces full swing output voltage.

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