IMPLEMENTATION OF LOW POWER AND AREA EFFICIENT SUM OF ABSOLUTE DIFFERENCE ARCHITECTURE USING BRENT KUNG ADDER

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***Abstract*: Sum of Absolute Difference is a popular technique for video encoding, however it is difficult to compute. The adder compressor is used to combine the fragmentary SAD value that is produced from the absolute difference of two video blocks. The high performance SAD architecture using an Brent Kung Adder is described in this paper. In digital circuits like multipliers, where several multi-bit operands must be added simultaneously, adder compressors have been widely employed. In this paper 8-2 adder compressor is designed and pipeline of eight 8-2 adder compressor is constructed, using Verilog HDL with different mixture for the recombination line. The output obtained from the simulation, schematic and synthesis show that Brent Kung Adder (BKA) is more effective and consumes less power then the other adder used in recombination line. The implementation of the design is done in Xilinx's Vivado 2018**

***keywords*: Adder compressor, BKA, SAD, Verilog HDL.**

I. INTRODUCTION

The most often used metric is sum of absolute difference (SAD), which has an adder-compressor and accumulator as part of its architecture. This is due to its simplicity and calculation efficiency. The bit adding process is carried out more quickly and effectively by the adder compressors. A multiplexer(MUX) and XOR logic blocks make up the adder compressor. To shorten the delay, a MUX is used to replace one of the compressor's XOR gates.. A 8:2 adder compressor is built using 12 XOR gates and 6 MUX. This can also be constructed by using 4-2 adder compressor and 3-2 adder compressor. 8:2 adder compressor has eight inputs (A,B,C,D,E,F,G,H), 5 Cin, 5 Cout, sum and carry. For the recombination line this paper consists of Brent Kung Adder (BKA), sum and carry of 8:2 adder compressor is given as the input for the brent kung adder and Cin=0 to obtain the results. The use of brent kung adder is to reduces the area and overall delay.

Using Verilog HDL, the codes are generated for adder compressor, pipeline of adder compressor and brent kung adder this are shown below. Implementing 8-2 adder compressor and constructing pipeline connection of eight 8-2 adder compressor. Understanding the working of Brent Kung Adder and Implementing. Developing a Verilog HDL code for the above.

For use in motion estimation in a mobile video coding system, a computationally effective architecture is given to compute the sum absolute difference (SAD) between two data sets. The benefits of the two earlier suggested architectures are combined and further promoted by the proposed architectures. As a result, compared to conventional architectures, more performance is obtained at reduced costs (number of ports and power consumption). Mobile video processing systems can incorporate the suggested architectures. They not only support all SAD criteria-based procedures but also conventional and data-independent motion estimate strategies. By including early termination techniques, the suggested design avoids calculations that would otherwise be necessary in traditional SAD systems without them.

One of the longest-running tasks of a video encoder compliant with a high-performance video encoding standard is sum absolute difference (SAD). The absolute difference between two image blocks is accumulated by the SAD hardware design via an additive tree. The many compressor adder constructs in the SAD hardware design are examined in this article. Standard 45 nm CMOS cells are used to synthesis the structures. According to the combined findings, the SAD design, which uses 82 compressors—42 of which are in the recombination line—and Kogge Stone adders, reduces power dissipation by an average of 25.5% when compared to the architecture. SAD utilizes a standard adder from a contemporary synthesis tool.

One of the calculations used to encode videos that takes the longest to complete is the Sum Absolute Difference (SAD). By combining the absolute values of the difference between two blocks of video pixels, the SAD operation is carried out. The effect of the absolute operator on the SAD architecture's power dissipation is demonstrated in this study. We study a number of methods for creating absolute operators in SAD systems that are designed to be energy efficient. The structures are contrasted with the reference compositor's absolute macro function.

II. METHODOLOGY

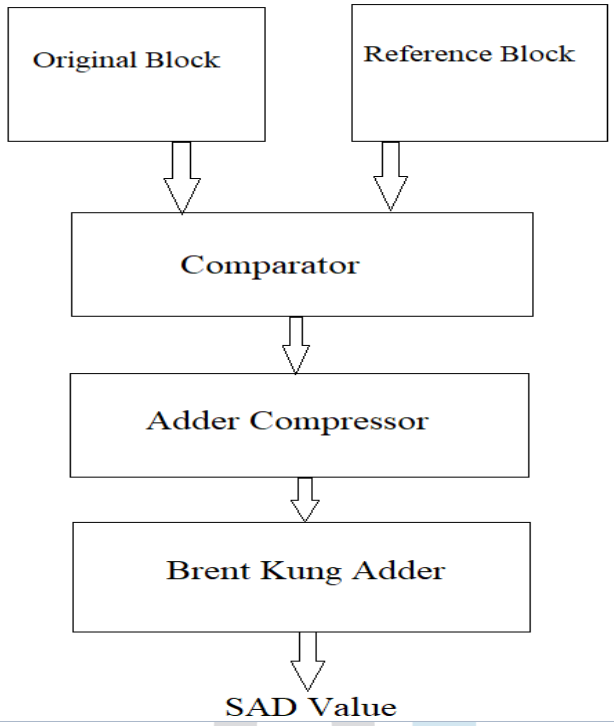


Fig 1: Flowchart for SAD architecture design

A 8-2 adder compressor takes 8bit number as input (a,b,c,d,e,f,g,h), 5bit cin (cin0,cin1,cin2,cin3,cin4) and gives output as sum, carry and 5bit cout (cout0,cout1,cout2,cout3,cout4).
The below fig2 shows the 8-2 adder compressor using xor gate and mux. A gate level Verilog HDL code is implemented for the below fig and verified using testbench.

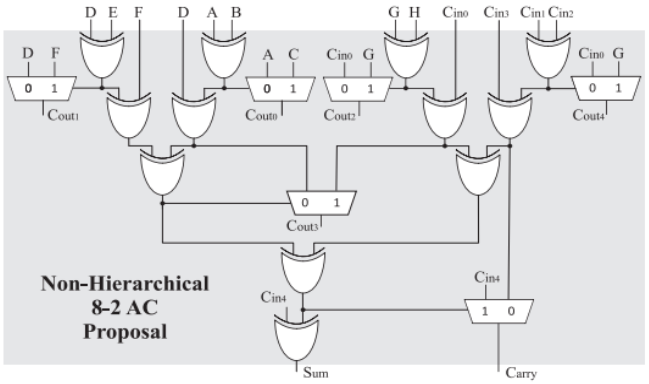


Fig 2: 8-2 Adder Compressor[1]

Pipeline connection of 8-2 adder compressor:

Eight primary and eight reference blocks, each 8 bits wide, are compared to one another for an 8x8 block size in a standard SAD architecture. Consequently, an adder compressor pipeline made up of eight, eight is to two adder compressors is required. As shown in the fig3.

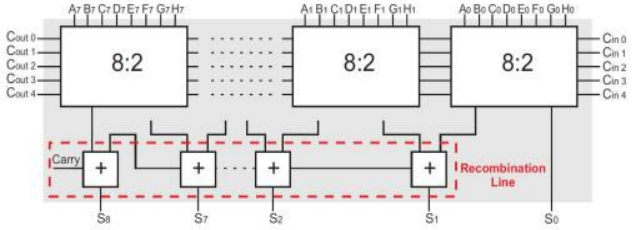


Fig 3: Pipeline of 8:2 Adder Compressor [1]

From the above fig, A to H are eight inputs to the design, each with an 8bit width. The module compressor_p is a single 8 is to 2 adder compressor which is constructed with the help of XOR gate and MUX as shown in the fig2. This (8-2) compressor is structurally modelled form the given structure. Verilog code is implemented for the pipeline. In the pipeline structure, the wires W1 to W35 are used for cary_in and carry_out for the next and previous adder compressor. There is a recombination line that employs a Brent Kung Adder. to combine the SAD partial values. BKA is used in this instance because it significantly increase the power efficiency of the SAD architecture, particularly when the compressor is comprised solely of an 8-2 adder compressor and BKA in the recombination line.

Brent Kung Adder:

A parallel prefix adder variation of a carry lookahead adder is the Brent Kung Adder. Compared to the kogge-stone adder, this has more regularity in the construction and less wire congestion, which improves performance and requires less area to implement. In comparison to ripple-carry adders, it is also more faster. Due of its speed relative to other adders, the Brent Kung Adder is more commonly used. The intermediate values are added using BKA, and then the carry from BKA and the output of the last compressor are added using a half adder to produce the MSB bit.

III. SCHEMATIC OF SAD:

To obtain the Sum of Absolute Difference, eight adder compressors and a Brent Kung adder are required. Waveforms and a netlist schematic were generated, certain test cases were provided to the test bench. Figures 4 and 5 below, which show the waveform and netlist schematic, respectively.

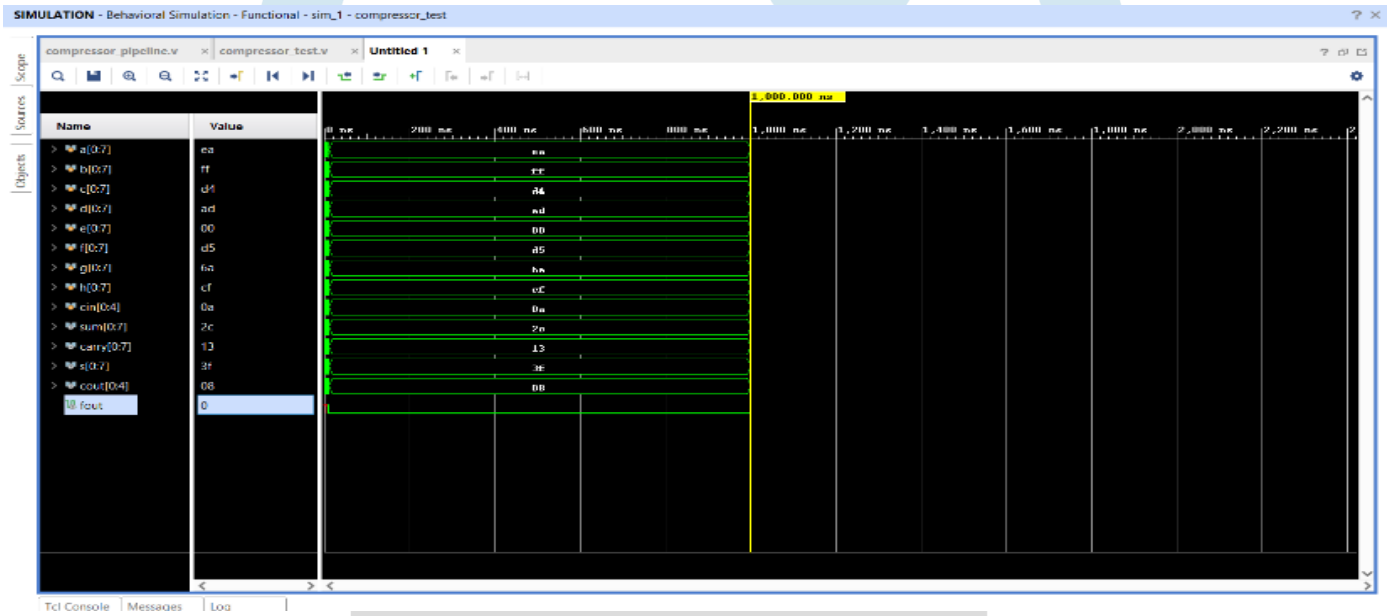
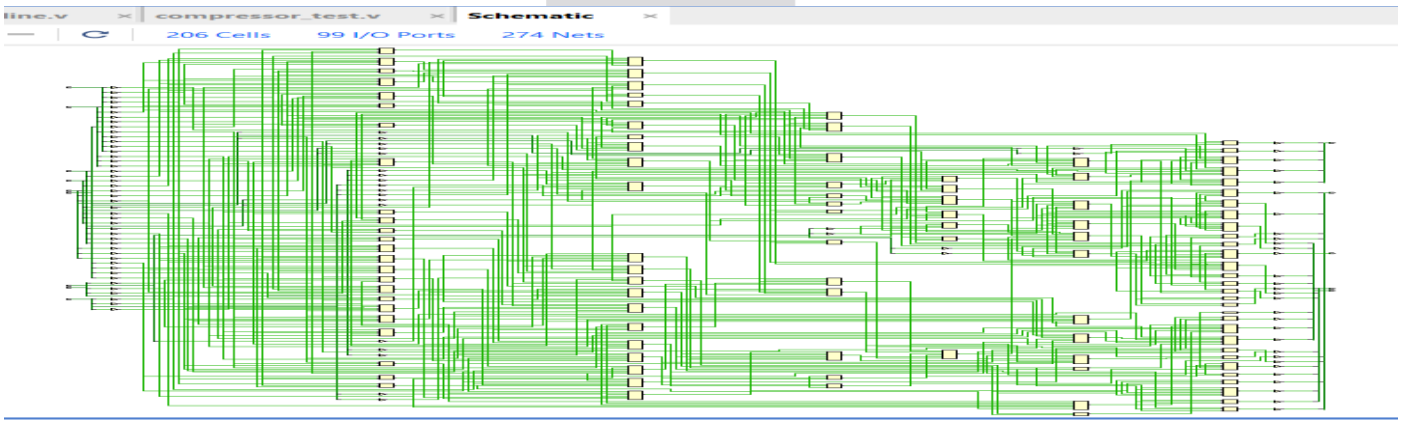


Fig 4: Simulation of SAD Architecture.

The above fig 4, shows the waveform of the SAD architecture, this are obtained from certain test values given in the test-bench.



The above fig 5, shows the schematic diagram of the SAD architecture, this is obtained from the run synthesis design.

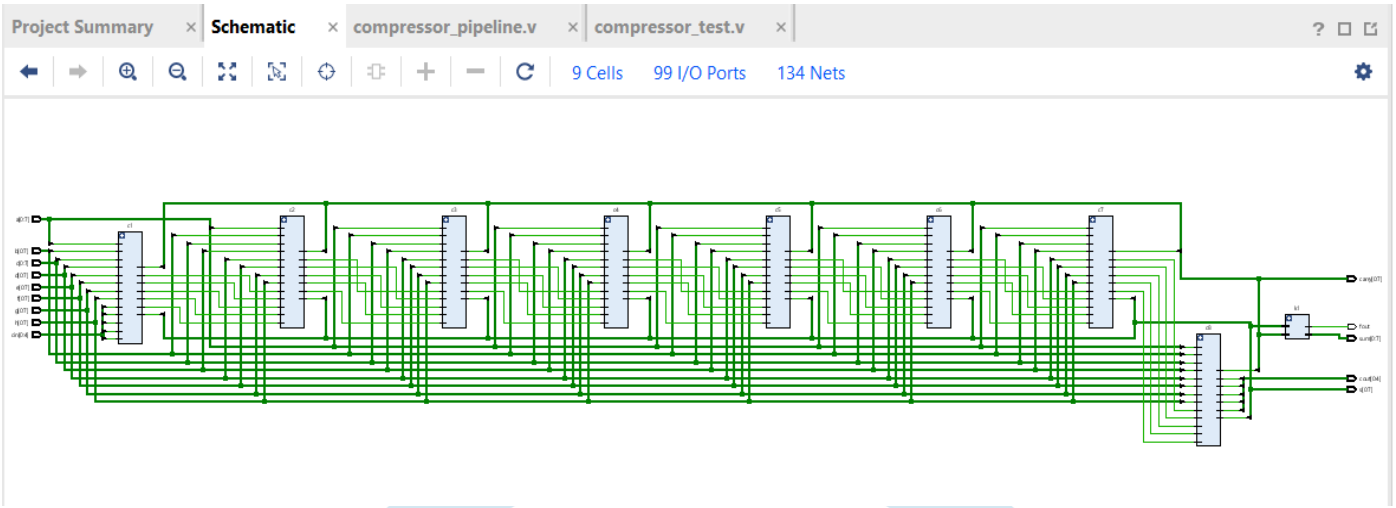


Fig 6: Schematic of SAD architecture generated on vivado.

The above fig 6, shows the schematic of SAD architecture, which is obtained from the Verilog code, this is also known as gate level netlist, this gate level netlist further given to the physical design.

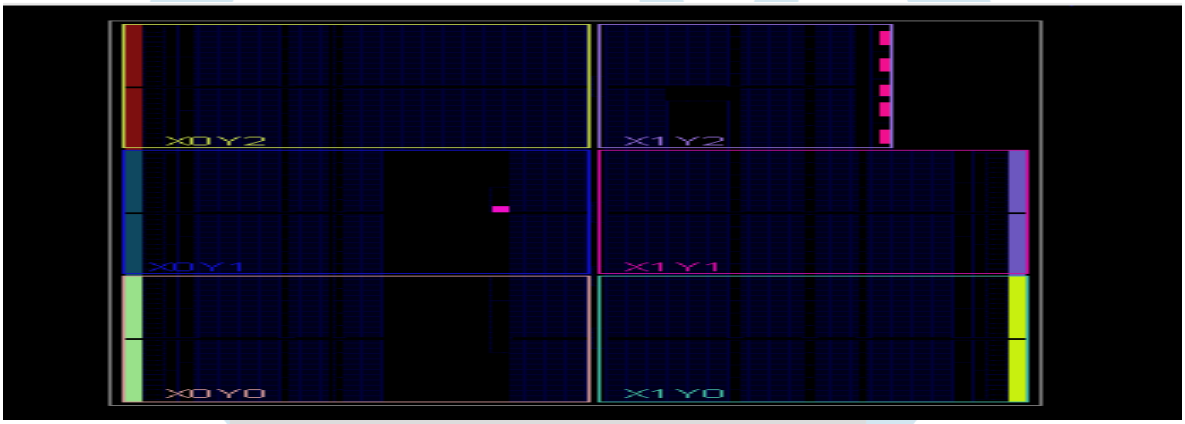


Fig 7: Device of SAD Architecture

I. RESULTS

The analysis of the designed SAD architecture provides high speed operation and low power consumption.

Area Report:

Instance	Cells	Cell Area	Net Area	Total Area	Wireload
compressor_pipeline	166	4344	0	4344	<none> (D)
k1	22	565	0	565	<none> (D)
h1	1	37	0	37	<none> (D)
c8	18	472	0	472	<none> (D)
m6	1	27	0	27	<none> (D)
m5	1	27	0	27	<none> (D)
m4	1	27	0	27	<none> (D)
m3	1	27	0	27	<none> (D)
m2	1	27	0	27	<none> (D)
m1	1	27	0	27	<none> (D)
c7	18	472	0	472	<none> (D)
m6	1	27	0	27	<none> (D)
m5	1	27	0	27	<none> (D)
m4	1	27	0	27	<none> (D)
m3	1	27	0	27	<none> (D)
m2	1	27	0	27	<none> (D)
m1	1	27	0	27	<none> (D)
c6	18	472	0	472	<none> (D)
m6	1	27	0	27	<none> (D)
m5	1	27	0	27	<none> (D)
m4	1	27	0	27	<none> (D)
m3	1	27	0	27	<none> (D)
m2	1	27	0	27	<none> (D)
m1	1	27	0	27	<none> (D)

Power Report:

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
compressor_pipeline	166	203.557	450032.802	450236.358
k1	22	24.135	97528.630	97552.765
h1	1	1.424	7293.648	7295.072
c1	18	22.428	37671.244	37693.672
m1	1	1.314	450.090	451.404
m2	1	1.314	883.433	884.748
m3	1	1.314	708.949	710.263
m4	1	1.314	1114.162	1115.476
m5	1	1.314	1893.140	1894.454
m6	1	1.314	3145.682	3146.997
c2	18	22.428	42987.113	43009.540
m1	1	1.314	992.637	993.951
m2	1	1.314	589.110	590.424
m3	1	1.314	906.857	908.172
m4	1	1.314	1280.643	1281.958
m5	1	1.314	1697.578	1698.892
m6	1	1.314	4678.313	4679.628

Table: Comparison of Different Adders

Recombination Adder	Area (um^2)	Leakage Power (uW)	Dynamic Power (uW)	Total Power (uW)
Ripple carry with mux-based full adder [1]	1522	14.8	1311.2	1326.0
Ripple-carry with full adder [1]	1531	14.8	1307.9	1322.7
Carry Select Adder [1]	1458	12.8	1062.6	1075.4
Carry Lookahead Adder [1]	1486	13.5	1138.3	1151.8
Kogge Stone Adder [1]	1462	12.3	1071.6	1083.9
Proposed Brent Kung Adder	4344	0.203	450.0	450.2

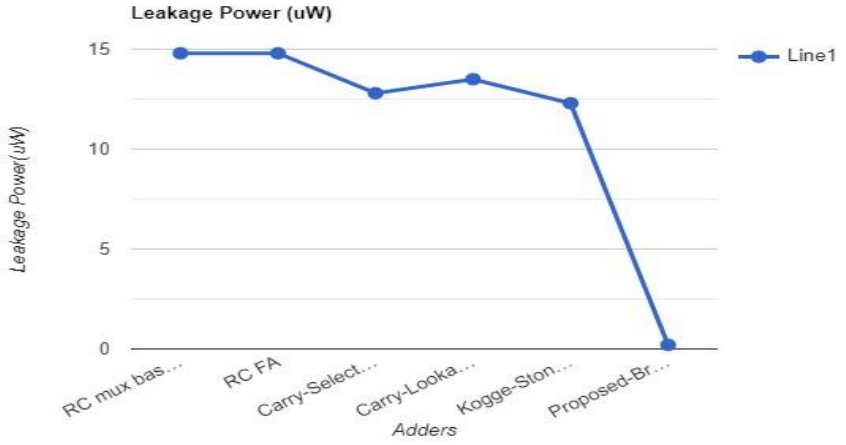


Fig: Leakage power of different Adders.

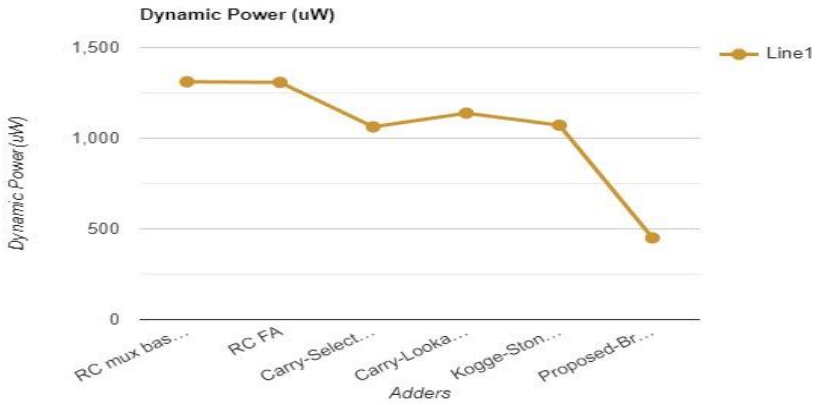


Fig: Dynamic power of different Adders.

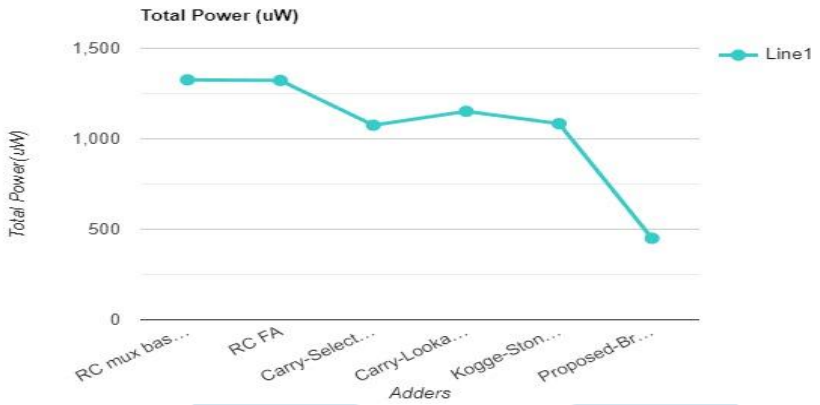


Fig: Total Power consumption of adders.

II. CONCLUSION:

The RTL netlist, gate level netlist, and waveform were obtained using Xilinx's Vivado 2018 software. This paper offers the Verilog HDL implementation of the SAD design. Brent Kung Adder is used in the SAD adder model because it is more efficient than other adders in the recombination line.

This paper outlines the fundamental steps for implementing the SAD architecture in Verilog for larger blocks, which uses less delay and power.

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