Design and Implementation of 45nm Operational Amplifier

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Abstract— Due to its extensive use of analog computation and signal processing, the operational amplifier is the most dominant device in the field of electronics. The main aim of this paper is to design and implement a two stage complementary metal oxide-semiconductor operational amplifier using required specifications. It also aims to examine the various results for various parameters. The simulation is carried out using Tanner tool which uses 45nm technology and the two stage metal oxide semiconductor operational amplifier runs on a supply voltage. Moreover the feasibility of this circuit is heavily dependent on the process variation, which has a significant advantage over analog circuits. As a result, various simulations including AC, DC and Temperature analysis have been carried out for validation additionally, specified gain of 80dB, Phase margin and power dissipation have also been carried out.

Index Terms—Two-stage Operational amplifier, Analog circuits, Gain, Power dissipation, Temperature analysis, Process variation

I. INTRODUCTION

All The Operational Amplifier is the Heart of any analog circuit, based on its design and functionalities the performance of entire circuit can be judged. It is a basic building block of analog and mixed signal circuits. Earlier, op amps were general purpose like IC 741 with compromise on the parameters such as output swing, power dissipation by contrast, now it’s possible to design op amp for specific need applications [1][2]. The modern op amp must operate at supply voltages as low as 0.9 volts while delivering single ended output swings as large as 0.8 volts, for instance, the gain and output swings provided by the cascode op amp are insufficient. Cascoding in one stage op amp increases the gain while limiting the output swings. In these scenarios, we switch to two-stage opamps[3][4], where the first stage provides high gain and the second stage provides large swings.

The key obstacle continues to be implementing two-stage CMOS Op-amps while taking other factors into consideration that constitute constraints. Here, the width to length ratio, or (W/L) ratio [6][7] is the main factor affecting the circuit's gain. However, a spike in gain is necessary for the goal of performance improvement and stability matching.

II. LITERATURE SURVEY

Ketan.J.Raut [6][7] represented the design of two stage op amp using standard 180nm technology and achieved the parameter gain of the amplifier is 74.89dB bandwidth is 7.3MHZ and the Slew rate is 94v/ms because of the high condensed slew rate it affects the amplifier. Chaitali et al. designed op amp in which transistors are operated for lower voltage low power applications using 180nm technology simulation has done. The circuit generates 40dB gain.

A. Problem Formulation:

Compared to analog circuit design, digital circuit design typically indicates increased automation. Analog sizing demands accurate modeling of the different sorts of parametric effects existing in a device because it is inherently information concentrated. Moreover, a traditional analog design challenge has more restrictions and occasionally involves complicated tradeoffs. However, because analog circuit level modifications allow for changes to the transistor level, the main structural component of a circuit, the analogue circuit level is significantly more important than its digital counterpart in terms of altering or improving a circuit's performance. The aspects promoted the use of analog design principles to design the operational amplifier, which again perform as an important component in many analog circuits, including integrators, differentiators, comparators, voltage followers, filters, and more.

B. Contribution of the Work:

In this Research, a systematic approach is used to Improve the precision with different variations that are conducted through experimental simulations of a two-stage OP Amp. The operational amplifier with 45nm technology will be used in the proposed method, and various simulations will be performed to understand about the operational amplifier's feasibility [1].

The Two-Stage operational amplifier consists of two stages. We use a Two-Stage op amp to get high gain and high output swing. Stage 2 is a PMOS common source amplifier with the optimal current source load.[4] where stage 1 is an Operational Amplifier with a single stage and gain, presuming that the M1 and M2 NMOS transistors, M3 and M4 PMOS transistors, Vin1 is inverting input and vin2 is non-inverting input. M6 and M7 are the common source amplifier A designer can choose the MOSFET'S length.
M3, M4, M6 have the same length whereas M3, M4 have same width and length, M5 and M8 forms NMOS current mirror have same length, M1 and M2 have same width and length 45nm technology depends on the performance of parameters such as (W/L) ratios to make the chip smaller[8][9].

III. METHODOLOGY

The design the operational amplifier for this research, we adopted 45nm technology. Various research were carried out to understand more about the operational amplifier’s effectiveness, or the circuit’s process variation. Various limitations have been taken into consideration. The node was constructed using 45nm technology, 1.8V was chosen as the voltage supply. In order to keep all MOS transistors in the saturation zone, the Input Common-Mode Range (ICMR) has been set between 0.8V and 1.6V, while the threshold voltages for nmos and pmos are 0.45V and 0.5V, respectively[2][4]. Similarly, 2PF has been chosen for the load capacitance so that the poles will remain before the 0dB point. This assures the circuit’s stability. For the optimal condition, the gain, slew rate, and gain-bandwidth product (GBW) have been selected. Here, maintaining the input voltage and output voltage swing within the ICMR range is crucial. The design process begins with research on exceptional Op-amp topologies that are frequently used [1][8].

The Design procedure of two stage Operational Amplifier specifications for following parameters are:

a) Voltage supply (VDD): 1.8V  
b) Gain (G) at dc: 80dB  
c) Gain bandwidth product (GBW): 30MHZ  
d) Input Common Mode Range (ICMR): 0.8V to 1.6V[V = vin(min) and vin(max)]  
e) Load Capacitance (C_L): 2pF  
f) Slew Rate (SR): \( \frac{20v}{\mu s} \)

**Calculation of compensation capacitor (C_L):**

For 80 degree phase margin, \( 0.22 \) (\( C_L = 0.44pF \))

**Selection of I_D5:**

Determining the min value for the tail current I_D5 based on Slew rate requirements \( I_D5 = SR(C_L) = 16\mu A \)

**Calculation of \( W_L(3,4) \):**

M3 is diode connected, \( V_{sg3} = V_{sd3} \). D3 & D1 are same where as \( V_{sd3} = V_{dd} \) & \( V_{d3} = V_{dd} \)

\( W/L)_3 = \frac{I_{ds}}{\mu p Cox(V_{dd} - V_{thn} - V_{thp})} \)

Thus W/L of M3 is determined by using max ICMR [Vin(max)].

\( W/L)_3 = \frac{I_{ds}}{\mu p Cox(V_{dd} - ICMR Max - V_{thd} + V_{thd})} \)

Approximately chooses as 14.

**Calculation of \( W_L(1,2) \):**

Size of M1 & M2 NMOS input transistors

Choose \( (W/L)_1 = \frac{(W/L)_2}{\mu p Cox I_{ds}} \) to achieve the desired dB

\( W/L)_1 = \frac{(W/L)_2}{\mu p Cox I_{ds}} \)

Approximately chooses as 6.

**Calculation of \( W_L(5,8) \):**

\( W/L)_5 = \frac{I_{ds}}{\mu p Cox(V_{dd})} \)

\( W/L)_5 = \frac{I_{ds}}{\mu p Cox(V_{dd})} \)

Approximately chooses as 12.

**Calculation of \( W_L(6) \):**

\( W/L)_6 = \frac{\mu p Cox(V_{dd})}{I_{ds}} \)

\( W/L)_6 = \frac{\mu p Cox(V_{dd})}{I_{ds}} \)

Approximately chooses as 180.

**Calculation of \( W_L(7) \):**

\( W/L)_7 = \frac{I_{ds}}{I_{ds}} \)

Where as \( I_{ds} = I_{ds} \)

Approximately chooses as 75.
The following figure demonstrates the two stage CMOS Op-amp schematic. The schematic is implemented using the calculated parameters that taken into consideration design requirements and specifications. Five NMOS and three PMOS constitute the operational amplifier with W/L values [5][8].

**Figure 1: Two Stage OP-amp**

**Figure 2: Schematic of Two stage Op-amp**

IV. RESULTS AND DISCUSSIONS

Before Using a Tanner tool and a 45nm node, the design and optimization of a two-stage CMOS Opamp circuit were verified. A supply voltage of 1.8V was used. To meet the various limitations of the circuit, multiple analysis including DC, AC, Transient, and Power analysis have been conducted [7][8].
**Transient Analysis:**

**DC Analysis:**

**Temperature Analysis:**
AC Analysis:

Power Results: temp=35
Total Power from time 0 to 0.001
Average power consumed -> 1.516047e+001 watts
Max power 1.516047e+001 at time 0.00027469
Min power 1.516047e+001 at time 0.000284687

Max power 1.660694e+001 at time 0.000446657
Min power 1.660694e+001 at time 0.000450067

Power Results: temp=30
Total Power from time 0 to 0.001
Average power consumed -> 1.633173e+001 watts
Max power 1.633173e+001 at time 0.000442567
Min power 1.633173e+001 at time 0.000428667

Power Results: temp=35
Total Power from time 0 to 0.001
Average power consumed -> 1.516047e+001 watts
Max power 1.516047e+001 at time 0.00027469
Min power 1.516047e+001 at time 0.000284687
Power Analysis

V. CONCLUSION

After For the two-stage Op-amp, Implementation is a multidimensional optimization problem where enhancing one or more parameters could actually deteriorate other Additionally, when designing circuits for high dc-gain and high bandwidth applications, the gain-bandwidth-product continually presents challenges to the designers[1]. As a result, the circuit modelling was carried out using a tanner tool with a 45nm node. The performance is enhanced by altering parameters like (W/L) ratios. Additionally, this makes use of design equations, including accurate selection and sizing of the proposed circuit's configuration. This proposed design achieves 80dB gain and phase margin at unity gain configuration and power dissipation[13][14].

VISI technology nodes such as 45nm came into existence and more would continue to come in future these technologies depends on the performance of parameters such as (W/L) ratios to make the chip smaller.

REFERENCES


