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In recognition of the publication of the paper entitled

**Low-Power 4A—4 Signed Multiplier Design Using Pass-Transistor Logic at 16nm
PTM**

Published in Volume 11 Issue 4, April-2026

*Co-Authors - Ch. Vinay, D. Vinay Kumar, C V P
Supradeepthi*

Paper ID - IJRTI2604194

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