Design of Tunnel FET and its Performance characteristics with various materials

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Abstract—In today’s technological environment, there is a huge demand for devices with low power and low cost storage space. Memories with low power are driving the entire VLSI industry as most of the devices work on remote power supply. Demand of low power becomes the key of VLSI designs rather than high speed, particularly in embedded SRAM’s and caches.

The tunneling field effect transistor uses the quantum mechanical generation of carriers by band-to-band tunneling. Tunneling FET meets the challenges like low Subthreshold Swing (SS), low supply voltage and lower leakage currents.

In particular, in this paper, we designed Tunnel FET with different materials such as Si and SiGe in different regions so as to produce low subthreshold swing, low leakage currents, low supply voltages and comparable \(I_{D-FF}\) and \(I_{ON}\). Idealized template devices were used to determine the device unidirectionality, which is inherent to TFETs. TFET with different material is used to investigate the \(V_{DD}\) range, in which TFETS may be advantageous when compared to conventional MOSFET. Ambipolarity of TFET was analyzed. Realistic device templates extracted from experimental data of fabricated state-of-the-art Silicon n-TFET was used to assess the performance gap between the simulation of idealized TFETs and the best experimental implementations with different materials

Index Terms— Tunneling-FET (TFET), sub threshold swing (SS), unidirectionality, leakage current Band to Band tunneling (BtBt).

I. INTRODUCTION

Now a day’s power consumption and size of the device are the main constraints. Tunnel-FET can replace or complement CMOSFET in Ultra Low Power (ULP) applications [1]. The TFET is a new type of transistor, its structure is similar to MOSFET but fundamental switching mechanism is different. TFET is made for low energy electrons. Tunnel FETs works on switching mechanism of modulating quantum tunneling through a barrier. Whereas MOSFET is modulating thermionic emission over a barrier. CMOS had a subthreshold swing is above or equal to 60mv/decade but TFET had a subthreshold swing below 60mv/decade at room temperature. In this thesis subthreshold swing of TFET demonstrated experimentally 30mv/decade or 25mv/decade. By using different materials various results were observed. By observing result obtained from different materials they can be used in SRAM as well as DRAM.

TFET had more impact on SRAM as SRAM can occupy 70% of processor area [2]. In advanced digital circuit’s important step should be taken to estimate the impact of using TFETs on the performance of SRAM.

Main intrinsic limitations of TFETs are asymmetry of Source(S) and Drain (D) regions that makes \(I_{D}\) inherently unidirectional this case is critical in SRAM. Band-to-Band tunneling (BtBt) is main concept in TFETs and this can increase drain current comparable to MOSFET.
- Low Subthreshold Swing (SS).
- Reduced leakage currents.
- Low applied voltage (\(V_{DD}\)).

II. TUNNELING FIELD EFFECT TRANSISTOR (TFET)

TFET device designed with single gate or double gate. In this particular concern double gate TFET was designed. TFET device consists of thin intrinsic silicon body and its thickness is denoted by \(T_{Si}\), source is highly doped p-type material and drain is moderately doped n-type material [3]–[5]. HfO\(_2\) and SiO\(_2\) are vertically extended to 5nm [included both]. The current flows from source to drain as opposite to electrons flow in the channel. The front gate and top gates of TFET are formed above and below the channel.

This is shown in Figure 1. The double gate present in TFET provides electrostatic control over the channel in which the drain field line cannot effect or disturb the channel and it significantly reduces the short channel effects. This type of design reduces the Leakage current as the second gate acts like the substrate [6]. The Double Gate Tunneling FET’s are of smaller dimension as
compared to the bulk type of transistors. To enhance the mobility ion transfer characteristic body is left un-doped. This type of design overcomes the drawbacks present in the conventional model.

Figure 1. Tunneling FET with source SiGe, drain and channel of Si material

The above figure 1 shows hetero-structure TFET in which source is SiGe material and channel and drain are of Si material at the top and bottom of gate was extended to 5nm of SiO$_2$ and HfO$_2$ which provides better electrical properties that is main objective of this paper. HfO$_2$ is high K-dielectric materials.

The following figure 2 is Silicon P-I-N structure TFET is a gated P-I-N diode where the source and drain are highly doped with the gate controlling the band-to-band tunneling between the I-channel region and the P+ or N+ region by way of energy band bending in the I-channel region. The gate induces an N+ channel to form at the surface of the I-channel region in this case and causes a P+/N+ junction to form at the source to channel interface. It has all three regions of Si, and the design procedure is same as hetero-structure TFET. Doping profiles are also same.

Figure 2. Silicon P-I-N structure TFET

III DEVICE DESIGN AND SIMULATION

This paper presents design of modified and effective Tunneling-FET in 30nm technology with different materials. That means by changing the drain, source and channel materials. In particular, in this paper we design both hetero structure TFET as well as simple Silicon P-I-N structure TFET. Due to the asymmetric nature of the P-I-N structure TFET, a self-aligned process similar to the process of a conventional MOSFET is not possible and the source and drain have to be formed separately. The P-I-N TFET process flow is developed using SOI wafers based on Sematech’s CMOS process flow using a high-k metal gate process. High-k materials with relative dielectric greater than 4 are used to reduce the leakage current and to increase the performance of the device. High-k materials used with Al as Gate are Al$_2$O$_3$, HfO$_2$, ZrO$_2$, TiO$_2$. These materials improve the performance after scaling.

When measuring these P-I-N structure TFETs, the diode behavior between the source and drain should always be measured to confirm the alignment of the source/drain implant half mask. All terminal current should be examined when measuring the $I_D$-$V_{GS}$ characteristics to measure real tunneling current. Processing of germanium has challenges such as achieving a good quality gate dielectric interface, dopant activation and ohmic contact to name a few. But germanium has been extensively researched as a replacement MOSFET channel material due to its higher mobility and many solutions to these processing challenges. Due to these benefits, utilizing germanium is explored to improve the performance of TFETs. Silicon/germanium hetero-structure TFETs are designed.

The Table 1 shows the properties of various materials used in the design of Tunneling-FET. As seen the relative dielectric values are generally more than 4 and up to a value of 80 for TiO$_2$. Also the Table details the comparison of several other electrical properties like thermal electrical conductivity, conductivity, specific heat and density.

As shown in Figure 1 source is made up of SiGe, channel and drain are made up of Si material. Figure2 shows that the Source and Drain made up of Silicon material and Gate is made up of Al material. The use of Al as Gate material it increases the current from Source to Drain. Since the gates are independent, it provides a better control in the variation of threshold voltage can be obtained.

Since the tunneling occurs mainly in the source to channel interface in the P-I-N structure TFET, reducing the band gap at this region would be most important for an increase in drive current. Thus we explore ways of using silicon and germanium hetero-structure at the source to channel interface and keep more silicon in the structure to utilize the developed baseline processes for
silicon. Source region in a silicon P-I-N is replaced with germanium which gives the benefit of the lower germanium band gap in the tunneling process but also keeps the benefit of good gate dielectric interface of silicon.

<table>
<thead>
<tr>
<th></th>
<th>SiO\textsubscript{2}</th>
<th>HfO\textsubscript{2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relative dielectric</td>
<td>3.90</td>
<td>25</td>
</tr>
<tr>
<td>Thermal Conductivity</td>
<td>1.38e+00</td>
<td>2.20E+01</td>
</tr>
<tr>
<td>(W/mK)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electrical Conductivity</td>
<td>1.00E-15</td>
<td>1.00E-12</td>
</tr>
<tr>
<td>(S/m)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Specific Heat</td>
<td>7.09E+02</td>
<td>2.61E+02</td>
</tr>
<tr>
<td>(J/kg K)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Density</td>
<td>2.20E+03</td>
<td>9.68E+03</td>
</tr>
<tr>
<td>(kg/m\textsuperscript{3})</td>
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Table 1: SiO\textsubscript{2} and HfO\textsubscript{2} dielectric materials comparison

As in the case of silicon P-I-N TFETs, some overlap between the gate and source is helpful in increasing the tunneling current. So an isotropic etch process needs to be developed that can remove the silicon in the source as well as under the gate. Etch recipes were developed to achieve a rounded shaped trench with gate overlap by using a two-step etch process. Since more vertical etch depth is needed compared to the lateral etch distance, a vertical anisotropic etch is first done followed by an isotropic etch.

The Tunneling FET using high-k materials can be used as high performance semiconductor devices. High-k dielectric materials remain at a low level even after extended operation of a transistor. The use of High-k material provides good electrical stability, and the amount of charge trapped in the high-k. The material used should be scalable as it provides an acceptable level of electron and hole mobility even at reduced thickness.

The thickness of the Gate Oxide material has to be increased to reduce leakage current. An alternative method to increase Gate Capacitance is replacing the relative dielectric constant of the material SiO\textsubscript{2} with a relatively high-k dielectric material. Leakage current can be used to reduce by the use of thicker dielectric Gate layer through the structure.

The sub-threshold swing (SS) of a device is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current. It can also define as the amount of gate voltage that is needed to bring down the subthreshold current by one decade. Both situations are considered one in strong inversion and other is considered in weak inversion.

IV RESULTS AND DISCUSSION

The electrical properties or characteristics of the Tunneling FETs were simulated for both Silicon P-I-N TFET structure as well as hetero-structure TFET by varying the device parameters. The device parameters used are: channel length L = 30nm, Silicon thickness t\textsubscript{Si} = 10nm, equivalent Gate Oxide thickness t\textsubscript{ox} = 1nm, L\textsubscript{sd} = 20nm and every time as per requirement there is change of dimensions take place in this particular concern. Channel region is intrinsic, doping concentration of the Source region N\textsubscript{A} = 10\textsuperscript{22} cm\textsuperscript{-3} and Drain region N\textsubscript{D} = 10\textsuperscript{20} cm\textsuperscript{-3}. The lateral length of the Source and Drain contacts were considered to be small (all most zero) for Silicon P-I-N TFET structure and hetero-structure TFET to avoid the influence of the series resistance on the I-V characteristics of TFET. The impact of high-k materials on the performance of Tunnel FET on both Silicon P-I-N TFET structure and hetero-structure TFET types is studied.

Hetero-structure TFET has more control over the device characteristics than the Silicon P-I-N TFET structure. The hetero junction was formed between source and channel i.e. at the edge of source region near the channel region. The simulation results proved that, the use of high-k materials in double gate as well as single gate Tunnel FETs has advantages like significantly reduced the leakage current and have given better controllability also gives the low subthreshold swing (SS).
The above figure 3 shows the $I_D$-$V_G$ curve for high-k dielectric material and different materials were used in different regions of the Tunnel FET. From the above graph we can infer that for low supply voltage the current is increased so that it can provide low subthreshold swing of below 60mv/decade. The increase in the gate voltage from 0v there is an increase in drain current.

In the figure 4 shows that $I_D$-$V_D$ as the drain voltage increases, higher electron density is formed in channel due to increase in the electric field along the position of the channel. By keeping front gate constant we can vary the drain voltage then the drain current increases drastically.

Figure 5 shows ON-current ($I_{ON}$) of Tunnel FET. As gate voltage ($V_G S$) changes from 0V to 0.5V then the ON-current ($I_{ON}$) decreases from maximum value of $2.6 \times 10^{-15}$ to minimum value $1.6 \times 10^{-15}$ by keeping drain voltage ($V_D$) at 0.5V.

Figure 6 shows the variation in the OFF-current ($I_{OFF}$). As the gate voltage changes from 0.7V to 1.5V, then the OFF-current changes from maximum value of $1.72 \times 10^{-15}$ to $1.94 \times 10^{-15}$. As shown in the figure 5&figure 6 the variation in the current ratio ($I_{ON}/I_{OFF}$) is determined with changes in gate voltage ($V_G S$).
Figure 7: \( I_D - V_{GS} \) of Tunneling FET (Npoly Si-Gate, \( V_{GS}=3V \), \( l=100nm, t_{ox}=2nm, L_{SP}=70nm, t_{il}=40nm \) at \( V_D=0.5V \). Figure 7 shows the characteristics of TFET with singe gate. As gate voltage increases from 0V to 3V the drain current increase, within small change in the gate voltage there is huge change in drain current. At gate voltage of \( V_{GS} \) the Subthreshold Swing (SS) is approximately 33mV/decade was achieved.

V. CONCLUSION

The simplest silicon P-I-N TFET structure and hetero-structure TFETs were designed with various materials and different dielectric materials like SiO2 and high-k material HfO2 (k~25) are used. The device performance was analyzed for different structures of TFET with various materials and the characteristics were analyzed. The Subthreshold Swing (SS) for each structure was determined, and it found to be below 60mV/decade with low the supply voltage (\( V_{DD} \)) which states that the Tunnel FET is very suitable for Ultra-Low Power (ULP) applications. The simulation results shows that the use of Tunnel FET can reduce supply voltage, subthreshold swing, leakage currents and improves current ratio (\( I_{ON}/I_{OFF} \)) and also gives the better performance.

References:
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